REALTEK WIRELESS LAN NETWORK INTERFACE CONTROLLER RTL8180

1. Features

- 128-Pin LQFP
- Supports descriptor-based buffer management
- Patented integrated Wireless LAN MAC and Direct Sequence Spread Spectrum Baseband Processor in one chip
- Enhanced Signal Detector
- Processing Gain FCC compliance
- On-Chip A/D and D/A converters for I/Q Data, AGC, and Adaptive Power Control
- Targeted for Multipath Delay Spreads 125ns at 11Mbps
- Supports Antenna Diversity
- 1 Mbps, 2 Mbps, 5.5 Mbps, and 11 Mbps operation
- PCI local bus network interface controller
  - Compliant to PCI Revision 2.2
  - Supports PCI clock 16.75MHz-40MHz
  - Supports PCI target fast back-to-back transaction
  - Supports Memory Read Line, Memory Read Multiple, Memory Write and Invalidate
  - Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8180's operational registers
  - Supports PCI VPD (Vital Product Data)
  - Supports ACPI, PCI power management
- Supports CardBus. The CIS can be stored in a 93C56.
- Supports 44MHz OSC as the internal clock source. The frequency deviation of OSC must be within 25 PPM.
- Compliant to PC97, PC98, PC99 and PC2001 standards
- Supports Wake-On-LAN (WOL) function and remote wake-up (Magic Packet* and Microsoft® wake-up frame)
- Supports 4 WOL signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, to be ready for remote wake-up when main power remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space
- Compliant to IEEE 802.11 and IEEE 802.11b standards
- Supports Short Preamble option
- Internal encryption/decryption engine executes IEEE 802.11 40 bits and 104 bits WEP
- Supports 11Mbps rates with automatic fallback to 5.5, 2, and 1Mbps
- Includes a programmable, PCI burst size and early Rx threshold
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
- Contains two large independent transmit and receive FIFO devices
- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) or 93C56 (128*16-bit EEPROM) to store resource configuration, ID parameter, and VPD data. The 93C56 can also be used to store the CIS data structure for CardBus applications.
- Supports LED pins for various network activity indications
- Supports 1 general purpose input pin and up to 3 general purpose output pins.
- Supports digital loopback capability on both ports
- Universal Chip for various Radio Front End for different applications
- Supports software control on 3-wire bus on RF chipset.
- 3.3V and 1.8V power supplies needed
- 5V tolerant I/Os
- 0.18µ CMOS process

2. General Description

The Realtek RTL8180 is a highly integrated and cost-effective wireless LAN network interface controller that integrates a wireless LAN MAC and a direct sequence spread spectrum baseband processor into one chip. It provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.11 and IEEE 802.11b specifications.

The RTL8180 has on board A/D and D/A converters for analog I and Q inputs and outputs. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with complementary code keying to provide a variety of data rates. Both receive and transmit AGC functions obtain maximum performance in the analog portions of the transceiver. The RTL8180 also includes a built-in enhanced signal detector to alleviate severe multipath effects. The target environment for 11Mbps is 125ns RMS delay spread. It also supports short preamble and antenna diversity. For security issues, the RTL8180 also implements a high performance internal WEP engine supporting up to 104 bit WEP.

It also supports Advanced Configuration Power management Interface (ACPI), PCI power management system for modern operating systems that are capable of Operating System directed Power Management (OSPM) to achieve the most efficient power management possible.

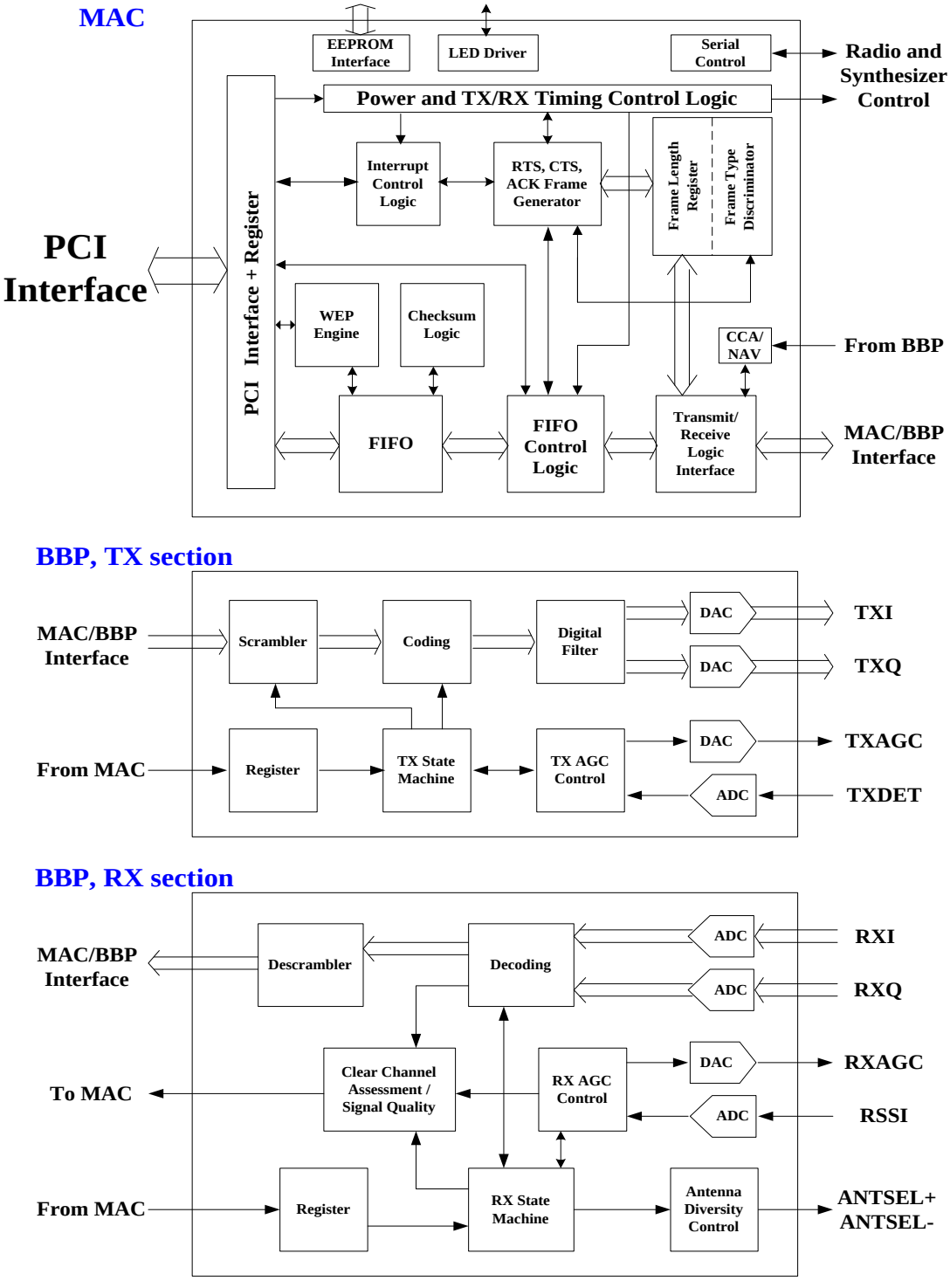
In addition to the ACPI feature, the RTL8180 also supports remote wake-up (including AMD Magic Packet and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8180 is capable of performing an internal reset through the application of auxiliary power. When the auxiliary power is applied and the main power remains off, the RTL8180 is ready and waiting for the Magic Packet or wake-up frame to wake the system up. Also, the LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8180 LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality.

PCI Vital Product Data (VPD) is also supported to provide the information that uniquely identifies hardware (i.e., the RTL8180 LAN card). The information may consist of part number, serial number, and other detailed information.

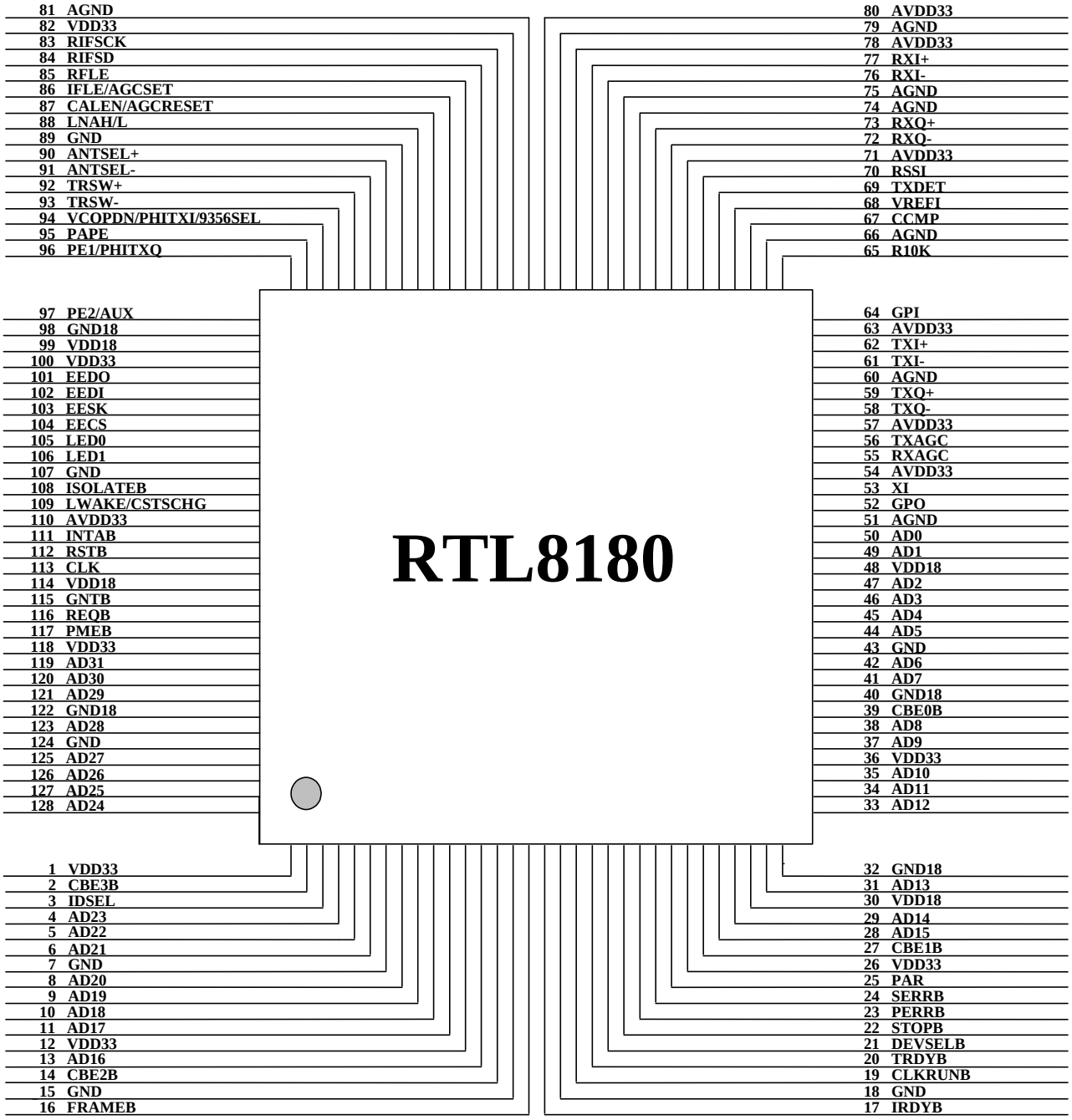
The RTL8180 supports an enhanced link list descriptor-based buffer management architecture, which is an essential part of a design for a modern network interface card. It contributes to lowering CPU utilization. Also, the RTL8180 boosts its PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving.

The RTL8180 keeps network maintenance costs low and eliminates usage barriers. The RTL8180 is highly integrated and requires no “glue” logic or external memory.

3. Block Diagram



4. Pin Assignments



5. Pin Descriptions

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the Pin Assignment diagram for a graphical representation.

5.1 Power Management/Isolation Interface

Symbol	Type	Pin No	Description
LWAKE/ CSTSCHG	O	109	**LAN WAKE-UP Signal** (When CardB_En=0, bit3 Config3): This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL) functionality. There are 4 choices of output, including active high, active low, positive pulse, and negative pulse, that may be asserted from the LWAKE pin. Please refer to the LWACT bit in the CONFIG1 register and the LWPTN bit in the CONFIG4 register for the setting of this output signal. The default output is an active high signal. Once there is a PME event having come in, the LWAKE and PMEB asserts at the same time when LWPME (bit4, CONFIG4) is set to 0. If LWPME is set to 1, LWAKE asserts only when PMEB asserts and ISOLATEB is low. **CSTSCHG Signal** (When CardB_En=1, bit3 Config3): This signal is used in CardBus applications only and is used to inform the motherboard to execute the wake-up process whenever a PME event occurs. This is always an active high signal, and the setting of LWACT (bit 4, Config1), LWPTN (bit2, Config4), and LWPME (bit4, Config4) means nothing in this case. This pin is a 3.3V signaling output pin.
ISOLATEB (ISOLATE#)	I	108	**Isolate Pin**: Active low. Used to isolate the RTL8180 from the PCI bus. The RTL8180 does not drive its PCI outputs (excluding PME#) and does not sample its PCI input (including RST# and PCICLK) as long as the Isolate pin is asserted.
PMEB (PME#)	O/D	117	**Power Management Event**: Open drain, active low. Used by the RTL8180 to request a change in its current power management state and/or to indicate that a power management event has occurred.

5.2 PCI Interface

Symbol	Type	Pin No	Description
AD31-0	T/S	119-121, 123, 125-128, 4-6, 8-11, 13, 28-29, 31, 33-35, 37-38, 41-42, 44-47, 49-50	**PCI Address and Data Multiplexed Pins**: The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, it is a double-word address. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted.
C/BE3-0	T/S	2, 14, 27, 39	**PCI Bus Command and Byte Enables Multiplexed Pins**: During the address phase of a transaction, C/BE3-0 defines the bus command. During the data phase, C/BE3-0 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0 applies to byte 0, and C/BE3 applies to byte 3.
CLK	I	113	**PCI Clock:** This clock input provides timing for all PCI transactions and is an input to the PCI device.
CLKRUNB	I/O	19	**Clock Run:** This signal is used by the RTL8180 to request starting (or speeding up) the clock, CLK. CLKRUNB also indicates the clock status. For the RTL8180, CLKRUNB is an open drain output as well as an input. The RTL8180 requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.
DEVSELB	S/T/S	21	**Device Select:** As a bus master, the RTL8180 samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8180 asserts this signal low when it recognizes its target address after FRAMEB is asserted.
FRAMEB	S/T/S	16	**Cycle Frame:** As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is deasserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNTB	I	115	**Grant:** This signal is asserted low to indicate to the RTL8180 that the central arbiter has granted ownership of the bus to the RTL8180. This input is used when the RTL8180 is acting as a bus master.
REQB	T/S	116	**Request**: The RTL8180 will assert this signal low to request the ownership of the bus to the central arbiter.
IDSEL	I	3	**Initialization Device Select**: This pin allows the RTL8180 to identify when configuration read/write transactions are intended for it.
INTAB	O/D	111	**Interrupt A:** Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask.

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IRDYB	S/T/S	17	**Initiator Ready**: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the RTL8180 is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	20	**Target Ready:** This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.
PAR	T/S	25	**Parity:** This signal indicates even parity across AD31-0 and C/BE3-0, including the PAR pin. PAR is stable and valid one clock after each address phase. For data phases, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
PERRB	S/T/S	23	**Parity Error:** This pin is used to report data parity errors during all PCI transactions except a Special Cycle. PERRB Is driven active (low) two clocks after a data parity error is detected by the device receiving data, and the minimum duration of PERRB is one clock for each data phase with parity error detected.
SERRB	O/D	24	**System Error:** If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, the RTL8180 asserts the SERRB pin low and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	22	**Stop:** Indicates that the current target is requesting the master to stop the current transaction.
RSTB	I	112	**Reset:** When RSTB is asserted low, the RTL8180 performs an internal system hardware reset. RSTB must be held for a minimum of 120 ns.

5.3 EEPROM Interface

Symbol	Type	Pin No	Description
EESK	O	103	EESK in 93C46 (93C56) programming or auto-load mode.
EEDI	O	102	EEDI in 93C46 (93C56) programming or auto-load mode.
EEDO	O/I	101	EEDO in 93C46 (93C56) programming or auto-load mode.
EECS	O	104	**EEPROM Chip Select:** 93C46 (93C56) chip select

5.4 Power Pins

Symbol	Type	Pin No	Description
VDD33	P	1, 12, 26, 36, 82, 100, 110, 118	**+3.3V (Digital)**
AVDD33	P	54, 57, 63, 71, 78, 80, 110	**+3.3V (Analog)**
VDD18	P	30, 48, 99, 114	**+1.8V**
GND	P	7, 15, 18, 43, 89, 107, 124	**Ground (Digital)**
AGND	P	51, 60, 66, 74, 75, 79, 81	**Ground (Analog)**
GND18	P	32, 40, 98, 122	**Ground (+1.8V)**

5.5 LED Interface

Symbol	Type	Pin No	Description
LED0, 1	O	105, 106	**LED pins** (Active low) **LEDS1-0** / **00** / **01** / **10** / **11** **LED0** / TX/RX / TX/RX / TX / LINK/ACT **LED1** / Infrastructure / LINK / RX / Infrastructure During power down mode, the LED signals are logic high.

5.6 Attachment Unit Interface

5.6.1 Intersil RF Chipset

Symbol	Type	Pin No	Description
RIFSCK	O	83	**3-wire Bus Clock**
RIFSD	O	84	**3-wire Bus Data**
RFLE	O	85	**3-wire Bus Enable**
IFLE/AGCSET	O	86	**IF_LE of the Intersil Chipset:** PLL Synthesizer Serial Interface Latch Enable Control. CMOS output.
CALEN/ AGCRESET	O	87	**CAL_EN of the Intersil Chipset:** CMOS output for activation of DC offset adjust circuit. A rising edge activates the calibration cycle, which completes within a programmable time and holds the calibration while this pin is held high. In applications where the synthesizer is not used, this pin needs to be grounded.
LNA_H/L	O	88	**Drive to the RF AGC Stage Attenuator:** CMOS digital.
ANTSEL+	O	90	**Antenna Select +:** The antenna selects signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL- for differential drive of antenna switches.
ANTSEL-	O	91	**Antenna Select -:** The antenna selects signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL+ for differential drive of antenna switches.
TRSW+ TRSW-	O O	92 93	**Transmit/Receive Control**
VCOPDN/ PHITXI/ 9356SEL	O/I	94	**Output Pin as VCO VCC Power Enable/Disable.** **Input Pin as 9356 Select Pin at Initial Power-up.** When this pin is pulled high with a 10KΩ resistor, the 93C56 EEPROM is used to store the resource data and CIS for the RTL8180. The RTL8180 latches the status of this pin at power-up to determine what EEPROM(93C46 or 93C56) is used.
PAPE	O	95	**Transmit PA Power EnableA**
PE1/PHITXQ	O	96	The combination of PE1 and PE2 are as follows: 00: Power Down State, PLL Registers in Save Mode, Inactive PLL, Active Serial 11: Receive State, Active PLL 10: Transmit State, Active PLL 01: Inactive Transmit and Receive States, Active PLL, Active Serial Interface
PE2/AUX	O/I	97	**Output Pin as PE2:** Refer to PE1 description. **Input Pin as Auxiliary Power Detect:** This pin is used to detect if Aux. Power exists, when initial power-on or PCI reset is de-asserted. Besides connecting this pin to EEPROM, it should be pulled high to the Aux. Power via a resistor to detect Aux. power. If this pin is not pulled high to Aux. Power, the RTL8180 assumes that no Aux. power exists. To support wakeup from ACPI, this pin must be pulled high to aux. power via a resistor.

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RXI+ RXI-	AI* AI	77 76	**Receive (Rx) In-phase Differential Analog Data**
RXQ+ RXQ-	AI AI	73 72	**Receive (Rx) Quadrature Differential Analog Data**
RSSI	AI	70	**Analog Input to the Receive Power A/D Converter for AGC Control**
TXDET	AI	69	**Input to the Transmit Power A/D Converter for Transmit AGC Control**
VREFI	AI	68	**Voltage Reference for ADC and DAC**
TXI+ TXI-	AO AO	62 61	**Transmit (TX) In-phase Differential Analog Data**
TXQ+ TXQ-	AO AO	59 58	**Transmit (TX) Quadrature Differential Analog Data**
TXAGC	AO	56	**Analog Drive to the Transmit IF Power Control**
RXAGC	AO	55	**Analog Drive to the Receive IF AGC Control**

*A=Analog signal

5.6.2 RFMD RF Chipset

Symbol	Type	Pin No	Description
RIFSCK	O	83	**3-wire Bus Clock:** The serial clock output, with resistive dividers on board to allow programming from +5V levels.
RIFSD	O	84	**3-wire Bus Data:** Serial data output, with resistive dividers on board to allow programming from +5V levels.
RFLE	O	85	**3-wire Bus Enable:** Enable serial port output, with resistive dividers on board to allow programming from +5V levels.
IFLE/AGCSET	X*	86	Not used in the RFMD RF chipset.
CALEN/ AGCRESET	X	87	Not used in the RFMD RF chipset.
LNA_H/L	O	88	**RF2494 Gain Select:** Digital output.
ANTSEL+	O	90	**Antenna Select +:** The antenna selects signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL- for differential drive of antenna switches.
ANTSEL-	X	91	Not used in the RFMD RF chipset.
TRSW+	X	92	Not used in the RFMD RF chipset.
TRSW-	X	93	Not used in the RFMD RF chipset.
VCOPDN/ PHITXI/ 9356SEL	O/I	94	**Output Pin as VCO VCC Power Enable/Disable.** **Input Pin as 9356 Select Pin at Initial Power-up:** When this pin is pulled high with a 10KΩ resistor, the 93C56 EEPROM is used to store the resource data and CIS for the RTL8180. The RTL8180 latches the status of this pin at power-up to determine what EEPROM (93C46 or 93C56) is used.
PAPE	O	95	**Power Control Output for RF2189 PA:** 0V to +3.3V.
PE1/PHITXQ	O	96	This pin is the shutdown control output on board regulator when the RF Module enters either power-saving or standby mode.
PE2/AUX	O/I	97	**Output pin as RF2948 RX EN/ TX EN, RF2494 OE and CE:** Refer to the RF2948 and RF2494 datasheets. **Input Pin as Auxiliary Power Detect:** This pin will detect if Aux. power exists, when initial power-on or PCI reset is de-asserted. Besides connecting this pin to EEPROM, it should be pulled high to the Aux. power via a resistor to detect Aux. power. If this pin is not pulled high to Aux. Power, the RTL8180 assumes there is no Aux. power. To support wakeup from ACPI, this pin must be pulled high to aux. power via a resistor.
RXI+	AI*	77	**Receive (Rx) In-phase Analog Data in Single Ended**
RXI-	X	76	Not used in RFMD RF chipset.
RXQ+	AI	73	**Receive (Rx) Quadrature-phase Analog Data in Single Ended**
RXQ-	X	72	Not used in RFMD RF chipset.
RSSI	X	70	Not used in RFMD RF chipset.
TXDET	AI	69	To internal ADC which detects transmit power.
VREFI	AI	68	Reference voltage for ADC, DAC from VREF1 of RF2948B.
TXI+	AO	62	**Transmit (TX) In-phase Digital Data:** Combining before connecting to TX_I of RF2948B.
TXI-	AO	61	
TXQ+	AO	59	**Transmit (TX) Quadrature Digital Data:** Combining before connecting to TX_Q of RF2948B.
TXQ-	AO	58	
TXAGC	AO	56	Transmit gain control output to RF2948.
RXAGC	AO	55	RF2948 VGC receiver gain control analog output.

*A=Analog signal
*X=Not used .

5.6.3 Philips RF Chipset

Symbol	Type	Pin No	Description
RIFSCK	O	83	**3-wire Bus Clock:** The pin RIFSCK is the "shift clock" output. If the 3-wire bus is enabled, address or data bits will be clocked out from the RIFSD pin with rising edges of RIFSCK.
RIFSD	O	84	**3-wire Bus Data:** The pin RIFSD is the output "data" pin. The detail timing is on 11.3.3.
RFLE	O	85	**3-wire Bus Enable:** The pin RFLE is an "enable" signal. It is level sensitive: If RFLE is of LOW value, the 3-wire bus interface on the SA2400 is enabled. This means that each rising edge on the RIFSCK pin will be taken as a shift cycle, and address/data bits are expected on RIFSD. If RFLE is HIGH, the 3-wire bus interface is disabled. No register settings will change regardless activity on RIFSCK and RIFSD.
IFLE/AGCSET	I	86	**AGCSET of the Philips Chipset:** On the digital output pin AGCRESET, a 0 => 1 transition clears AGCSET of SA2400 to logic 0 and SA2400 starts the AGC cycle. At end of AGC cycle, the AGCSET of SA2400 is asserted to logic 1. Then, AGCRESET will return to logic low.
CALEN/ AGCRESET	O	87	**AGCRESET of the Philips Chipset:** Please refer to the AGCSET description and Philips SA2400 datasheet.
LNA_H/L	X*	88	Not used in Philips RF chipset.
ANTSEL+	O	90	**Antenna Select +:** The antenna selects signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL- for differential drive of antenna switches.
ANTSEL-	O	91	**Antenna Select -:** The antenna selects signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL+ for differential drive of antenna switches.
TRSW+	O	92	**Transmit and Receive Switch Control:** This is a complement for TRSW-. 1:TX 0:RX
TRSW-	O	93	**Transmit and Receive Switch Control:** This is a complement for TRSW+. 1:RX 0:TX
VCOPDN/ PHITXI/ 9356SEL	O/I	94	**Output Pin as Transmit (TX) In-phase Digital Data of the Philips Chipset.** This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program). **Input Pin as 9356 Select Pin at Initial Power-up:** When this pin is pulled high with a 10KΩ resistor, the 93C56 EEPROM is used to store the resource data and CIS for the RTL8180. The RTL8180 latches the status of this pin at power-up to determine what EEPROM (93C46 or 93C56) is used.

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PAPE	O	95	**Transmit PA Power Enable:** Assert high when starting transmission.
PE1/PHITXQ	O	96	**Transmit (TX) Quadrature Digital Data of Philips Chipset.** This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
PE2/AUX	O/I	97	**Output Pin as TX/RX Control:** 1:RX 0:TX **Input Pin as Auxiliary Power Detect:** This pin detects the existence of Aux. Power, when initial power-on or PCI reset is de-asserted. Besides connecting this pin to the EEPROM, it should be pulled high to the Aux. Power via a resistor to detect Aux. power. If this pin is not pulled high to Aux. Power, the RTL8180 assumes there is no Aux. power. In addition, to support wakeup from ACPI, this pin must be pulled high to Aux. power via a resistor.
RXI+	AI*	77	**Receive (Rx) In-phase Analog Data:** Positive path of differential pair.
RXI-	AI	76	**Receive (Rx) In-phase Analog Data:** Negative path of differential pair.
RXQ+	AI	73	**Receive (Rx) Quadrature-phase Analog Data:** Positive path of the differential pair.
RXQ-	AI	72	**Receive (Rx) Quadrature-phase Analog Data:** Negative path of the differential pair.
RSSI	AI	70	**Received Signal Strength Indication:** To internal ADC.
TXDET	AI	69	**Transmit Power Detect:** To internal ADC which detects transmit power.
VREFI	AI	68	**Reference Voltage for ADC & DAC**
TXI+	AO	62	**Transmit (Tx) In-phase Analog Data:** Positive path of differential pair. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXI-	AO	61	**Transmit (Tx) In-phase Analog Data:** Negative path of differential pair. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXQ+	AO	59	**Transmit (Tx) Quadrature-phase Analog Data:** Positive path of the differential pair. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXQ-	AO	58	**Transmit (Tx) Quadrature-phase Analog Data:** Negative path of the differential pair. This function is valid on Tx digital mode (AnalogPhy = Digital on EEPROM writer program).
TXAGC	X	56	Not used in Philips RF chipset
RXAGC	X	55	Not used in Philips RF chipset

*A=Analog signal
*X=Not used .

5.7 Test, Clock and Other Pins

Symbol	Type	Pin No	Description
CCMP	I/O	67	**Compensation Capacitor:** This pin must be pulled high to VDD33 by a 0.1μF capacitor.
R10K	I/O	65	This pin must be pulled low by a 10K Ω resistor.
GPI	I	64	**General Purpose Input**
GPO	O	52	**General Purpose Output**
XI	I	53	**44 MHz OSC Input**

6. Register Descriptions

The RTL8180 provides the following set of operational registers mapped into PCI memory space or I/O space.

Offset	R/W	Tag	Description
0000h	R/W	IDR0	**ID Register 0:** The ID register0-5 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from EEPROM MAC Address field.
0001h	R/W	IDR1	**ID Register 1**
0002h	R/W	IDR2	**ID Register 2**
0003h	R/W	IDR3	**ID Register 3**
0004h	R/W	IDR4	**ID Register 4**
0005h	R/W	IDR5	**ID Register 5**
0006h-0007h	-	-	**Reserved**
0008h	R/W	MAR0	**Multicast Register 0:** The MAR register0-7 are only permitted to write by 4-bye access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers.
0009h	R/W	MAR1	**Multicast Register 1**
000Ah	R/W	MAR2	**Multicast Register 2**
000Bh	R/W	MAR3	**Multicast Register 3**
000Ch	R/W	MAR4	**Multicast Register 4**
000Dh	R/W	MAR5	**Multicast Register 5**
000Eh	R/W	MAR6	**Multicast Register 6**
000Fh	R/W	MAR7	**Multicast Register 7**
0010h-0017h	-	-	**Reserved**
0018h-001Fh	R	TSFTR	**Timing Synchronization Function Timer Register**
0020h-0023h	R/W	TLPDA	**Transmit Low Priority Descriptors Start Address** (32-bit). (256-byte alignment)
0024h-0027h	R/W	TNPDA	**Transmit Normal Priority Descriptors Start Address** (32-bit). (256-byte alignment)
0028h-002Bh	R/W	THPDA	**Transmit High Priority Descriptors Start Address (32-bit).** (256-byte alignment)
002Ch-002Dh	R/W	BRSR	**Basic Rate Set Register**
002Eh-0033h	R/W	BSSID	**Basic Service Set ID**
0034h-0036h	-	-	**Reserved**
0037h	R/W	CR	**Command Register**
0038h-003Bh	-	-	**Reserved**
003Ch-003Dh	R/W	IMR	**Interrupt Mask Register**
003Eh-003Fh	R/W	ISR	**Interrupt Status Register**
0040h-0043h	R/W	TCR	**Transmit (Tx) Configuration Register**
0044h-0047h	R/W	RCR	**Receive (Rx) Configuration Register**
0048h-004Bh	R/W	TimerInt	**Timer Interrupt Register.** Once having written a nonzero value to this register, the Timeout bit of ISR register will be set whenever the least 32 bits of the TSFTR reaches to this value. The Timeout bit will never be set as long as TimerInt register is zero.
004Ch-004Fh	R/W	TBDA	**Transmit Beacon Descriptor Start Address** (32-bit) (256-byte alignment)
0050h	R/W	9346CR	**93C46 (93C56) Command Register**
0051h	R	CONFIG0	**Configuration Register 0**
0052h	R/W	CONFIG1	**Configuration Register 1**
0053h	R/W	CONFIG2	**Configuration Register 2**
0054h-0057h	R/W	ANA_PARM	**Analog parameter**
0058h	R/W	MSR	**Media Status Register**
0059h	R/W	CONFIG3	**Configuration Register 3**
005Ah	R/W	CONFIG4	**Configuration Register 4**

Cont…

005Bh	R/W	TESTR	**TEST mode Register**
005Ch-005Dh	-	-	**Reserved**
005Eh	R/W	PSR	**Page Select Register**
005Fh	R/W	SCR	**Security Configuration Register**
0060h-006Fh	-	-	**Reserved**
0070h-0071h	R/W	BcnItv	**Beacon Interval Register**
0072h-0073h	R/W	AtimWnd	**Atim Window Register**
0074h-0075h	R/W	BintrItv	**Beacon interrupt Interval Register**
0076h-0077h	R/W	AtimtrItv	**Atim interrupt Interval Register**
0078h	R/W	PhyDelay	**Phy Delay Register**
0079h	R/W	CRCount	**Carrier Sense Counter**
007Ah-007Bh	-	-	**Reserved**
007Ch	R/W	PhyAddr	**Address register for Phy interface**
007Dh	W	PhyDataW	**Write Data to Phy**
007Eh	R	PhyDataR	**Read Data from Phy**
0080h-0083h	R/W	PhyCFG	**Phy Configuration Register**
0084h-00D3h is slected to page 1 when PSEn bit (bit 0, PSR) is set to 1			
0084h–008Bh	R/W	Wakeup0	**Power Management wakeup frame0 (64-bit)**
008Ch–0093h	R/W	Wakeup1	**Power Management wakeup frame1 (64-bit)**
0094h–009Bh	R/W	Wakeup2LD	**Power Management wakeup frame2 (128-bit), low D-Word**
009Ch–00A3h	R/W	Wakeup2HD	**Power Management wakeup frame2, high D-Word**
00A4h–00ABh	R/W	Wakeup3LD	**Power Management wakeup frame3 (128-bit), low D-Word**
00ACh–00B3h	R/W	Wakeup3HD	**Power Management wakeup frame3, high D-Word**
00B4h–00BBh	R/W	Wakeup4LD	**Power Management wakeup frame4 (128-bit), low D-Word**
00BCh–00C3h	R/W	Wakeup4HD	**Power Management wakeup frame4, high D-Word**
00C4h-00C5h	R/W	CRC0	**16-bit CRC of wakeup frame 0**
00C6h-00C7h	R/W	CRC1	**16-bit CRC of wakeup frame 1**
00C8h-00C9h	R/W	CRC2	**16-bit CRC of wakeup frame 2**
00CAh-00CBh	R/W	CRC3	**16-bit CRC of wakeup frame 3**
00CCh-00CDh	R/W	CRC4	**16-bit CRC of wakeup frame 4**
00CEh-00D3h	-	-	**Reserved**
0084h-00D3h is slected to page 0 when PSEn bit (bit 0, PSR) is set to 0			
0084h-008Fh	R/W	-	**Reserved**
0090h-009Fh	R/W	DK0	**Default Key 0 Register**
00A0h-00AFh	R/W	DK1	**Default Key 1 Register**
00B0h-00Bfh	R/W	DK2	**Default Key 2 Register**
00C0h-00CFh	R/W	DK3	**Default Key 3 Register**
00D0h-00D3h	-	-	**Reserved**
00D4h-00D7h	-	-	**Reserved**
00D8h	R/W	CONFIG5	**Configuration Register 5**
00D9h	W	TPPoll	**Transmit Priority Polling Register**
00DAh-00DBh	-	-	**Reserved**
00DCh-00DDh	R	CWR	**Contention Window Register**
00DEh	R	RetryCTR	**Retry Count Register**
00DFh-00E3h	-	-	**Reserved**
00E4h-00E7h	R/W	RDSAR	**Receive Descriptor Start Address Register (32-bit) (256-byte alignment)**
00E8h-00EFh	-	-	**Reserved**
00F0h-00F3h	R/W	FER	**Function Event Register (CardBus only)**
00F4h-00F7h	R/W	FEMR	**Function Event Mask Register (CardBus only)**
00F8h-00FBh	R	FPSR	**Function Present State Register (CardBus only)**
00FCh-00FFh	W	FFER	**Function Force Event Register (CardBus only)**

6.1 TSFTR: Timing Synchronization Function Timer Register (Offset 0018h-001Fh, R)

Bit	R/W	Symbol	Description
63:0	R	TSFT	**Timing Synchronization Function Timer:** RTL8180 maintain a TSF timer with modules 2^64 counting in increments of microseconds. The 8 octets are the timestamp field of beacon and probe response frame.

6.2 BRSR: Basic Rate Set Register (Offset 002Ch-002Dh, R/W)

Bit	R/W	Symbol	Description
15:9	-	-	**Reserved**
8	R/W	BPLCP	**0:Long PLCP header for CTS/ACK packet.** **1:Short PLCP header for CTS/ACK packet.**
7:2	-	-	**Reserved**
1:0	R/W	MBR	**Maximum Basic Service Set Basic Rate:** These bits indicate the highest BSS basic rate. All control frames shall be transmitted at the rate that is less than or equal to the maximum BSS basic Rate.

	Bit 1	Bit 0
1 Mbps	0	0
2 Mbps	0	1
5.5 Mbps	1	0
11 Mbps	1	1

6.3 BSSID: Basic Service Set ID (Offset 002Eh-0033h, R/W)

Bit	R/W	Symbol	Description
47:0	R/W	BSSID	**Basic Service Set Identification:** This register is written to by the driver after a NIC joins a network or creates an adhoc network.

6.4 CR: Command Register

(Offset 0037h, R/W)

This register is used for issuing commands to the RTL8180. These commands are issued by setting the corresponding bits for the function. A global software reset along with individual reset and enable/disable for transmitter and receiver are provided here.

Bit	R/W	Symbol	Description
7:5	-	-	**Reserved**
4	R/W	RST	**Reset:** Setting this bit to 1 forces the RTL8180 to a software reset state which disables the transmitter and receiver, and reinitializes the FIFOs. The values of IDR0-5 and MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8180 when the reset operation is complete.
3	R/W	RE	**Receiver Enable:** When set to 1, and the receive state machine is idle, the receive machine becomes active. This bit will read back as 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit. 1: Enable 0: Disable
2	R/W	TE	**Transmitter Enable:** When set to 1, and the transmit state machine is idle, the transmit state machine becomes active. This bit will read back as 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit. 1: Enable 0: Disable
1	-	-	**Reserved**
0	R/W	MulRW	**PCI Multiple Read/Write Enable:** 1: Enable 0: Disable

6.5 IMR: Interrupt Mask Register (Offset 003Ch-003Dh, R/W)

This register masks the interrupts that can be generated from the Interrupt Status Register. A hardware reset will clear all mask bits. Setting a mask bit allows the corresponding bit in the Interrupt Status Register to cause an interrupt. The Interrupt Status Register bits are always set to 1 if the condition is present, regardless of the state of the corresponding mask bit.

Bit	R/W	Symbol	Description
15	R/W	TXFOVW	**Tx FIFO Overflow Interrupt:** 1: Enable 0: Disable
14	R/W	TimeOut	**Time Out Interrupt:** 1: Enable 0: Disable
13	R/W	BcnInt	**Beacon Time out Interrupt:** 1: Enable 0: Disable
12	R/W	ATIMInt	**ATIM Time Out Interrupt:** 1: Enable 0: Disable
11	R/W	TBDER	**Tx Beacon Descriptor Error Interrupt:** 1: Enable 0: Disable
10	R/W	TBDOK	**Tx Beacon Descriptor OK Interrupt:** 1: Enable 0: Disable
9	R/W	THPDER	**Tx High Priority Descriptor Error Interrupt:** 1: Enable 0: Disable
8	R/W	THPDOK	**Tx High Priority Descriptor OK Interrupt:** 1: Enable 0: Disable
7	R/W	TNPDER	**Tx Normal Priority Descriptor Error Interrupt:** 1: Enable 0: Disable
6	R/W	TNPDOK	**Tx Normal Priority Descriptor OK Interrupt:** 1: Enable 0: Disable
5	R/W	RXFOVW	**Rx FIFO Overflow Interrupt:** 1: Enable 0: Disable
4	R/W	RDU	**Rx Descriptor Unavailable Interrupt:** 1: Enable 0: Disable
3	R/W	TLPDER	**Tx Low Priority Descriptor Error Interrupt:** 1: Enable 0: Disable
2	R/W	TLPDOK	**Tx Low Priority Descriptor OK Interrupt:** 1: Enable 0: Disable
1	R/W	RER	**Rx Error Interrupt:** 1: Enable 0: Disable
0	R/W	ROK	**Rx OK Interrupt:** 1: Enable 0: Disable

6.6 ISR: Interrupt Status Register (Offset 003Eh-003Fh, R/W)

This register indicates the source of an interrupt when the INTA pin goes active. Enabling the corresponding bits in the Interrupt Mask Register (IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one of more bits in this register are set to a "1". The interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Reading the ISR clears all interrupts. Writing a 1 to any bit in this register will reset that bit.

Bit	R/W	Symbol	Description
15	R/W	TXFOVW	**Tx FIFO Overflow**
14	R/W	TimeOut	**Time Out:** This bit is set to 1 when the least 32 bits of the TSFTR register reaches to the value of the TimerInt register.
13	R/W	BcnInt	**Beacon Time Out Interrupt:** When set, this bit indicates that the TBTT (Target Beacon Transmission Time) has been reached after the value of the Beacon interrupt Interval register.
12	R/W	ATIMInt	**ATIM Time Out Interrupt:** When set, this bit indicates that the ATIM window has been gone after the value of the Beacon interrupt Interval register.
11	R/W	TBDER	**Transmit Beacon Priority Descriptor Error:** Indicates that a packet of beacon priority descriptor transmission was aborted due to an Rx beacon frame.
10	R/W	TBDOK	**Transmit Beacon Priority Descriptor OK:** Indicates that a packet of beacon priority descriptor exchange sequence has been successfully completed.
9	R/W	THPDER	**Transmit High Priority Descriptor Error:** Indicates that a packet of high priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) has reached SRL (Short Retry Limit), and an SLRC (Station Long Retry Count) has reached LRL (Long Retry Limit).
8	R/W	THPDOK	**Transmit High Priority Descriptor OK:** Indicates that a packet of high priority descriptor exchange sequence has been successfully completed.
7	R/W	TNPDER	**Transmit Normal Priority Descriptor Error:** Indicates that a packet of normal priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) has reached SRL (Short Retry Limit), and an SLRC (Station Long Retry Count) has reached LRL (Long Retry Limit).
6	R/W	TNPDOK	**Transmit Normal Priority Descriptor OK:** Indicates that a packet of normal priority descriptor exchange sequence has been successfully completed.
5	R/W	FOVW	**Rx FIFO Overflow:** This bit set to 1 is caused by RDU, poor PCI performance, or overloaded PCI traffic.
4	R/W	RDU	**Rx Descriptor Unavailable:** When set, this bit indicates that the Rx descriptor is currently unavailable.
3	R/W	TLPDER	**Transmit Low Priority Descriptor Error:** Indicates that a packet of low priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) has reached SRL (Short Retry Limit), and an SLRC (Station Long Retry Count) has reached LRL (Long Retry Limit).
2	R/W	TLPDOK	**Transmit Low Priority Descriptor OK:** Indicates that a packet of low priority descriptor exchange sequence has been successfully completed.
1	R/W	RER	**Receive Error:** Indicates that a packet has a CRC32 or ICV error.
0	R/W	ROK	**Receive OK:** In normal mode, indicates the successful completion of a packet reception.

6.7 TCR: Transmit Configuration Register (Offset 0040h-0043h, R/W)

This register defines the Transmit Configuration for the RTL8180. It controls such functions as Loopback, Heartbeat, Auto Transmit Padding, programmable Interframe Gap, Fill and Drain Thresholds, and maximum DMA burst size.

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>31</td><td>R/W</td><td>CWMIN</td><td>Contention Window minimum value: Set to 1 to indicate that Cwmin=8. Set to 0 to indicate that Cwmin=32.</td></tr>
<tr><td>30</td><td>R/W</td><td>SWSEQ</td><td>Software Sequence Number:
1: Sequence number in WLAN header remains with software setting.
0: Hardware automatically updates sequence number in WLAN header.</td></tr>
<tr><td>29:25</td><td>R</td><td>HWVERID</td><td>Hardware Version ID:
<table>
<tr><th></th><th>Bit 29</th><th>Bit 28</th><th>Bit27</th><th>Bit26</th><th>Bit25</th></tr>
<tr><td>RTL8180</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="5">All other combinations</td></tr>
</table></td></tr>
<tr><td>24</td><td>R/W</td><td>SAT</td><td>Set ACK Timeout: The EIFS, ACK and CTS timeouts are derived from the following equation:
EIFS = 112/ACKrate + 252
1: ACKrate is dependent on the maximum of MBR (bits 1:0, BRSR) and Rx DATA/RTS rate.
0: ACKrate is fixed at 1Mbps.</td></tr>
<tr><td>23:21</td><td>R/W</td><td>MXDMA2, 1, 0</td><td>Max DMA Burst Size per Tx DMA Burst: This field sets the maximum size of transmit DMA data bursts according to the following table:
<table>
<tr><td>000: 16 bytes</td><td>100: 256 bytes</td></tr>
<tr><td>001: 32 bytes</td><td>101: 512 bytes</td></tr>
<tr><td>010: 64 bytes</td><td>110: 1024 bytes</td></tr>
<tr><td>011: 128 bytes</td><td>111: 2048 bytes</td></tr>
</table></td></tr>
<tr><td>20</td><td>R/W</td><td>DISCW</td><td>Disable Contention Window Backoff: This bit indicates the existence of a backoff procedure during packet transmission.
1: No random backoff procedure
0: Uses IEEE 802.11 random backoff procedure</td></tr>
<tr><td>19</td><td>R/W</td><td>ICV</td><td>Append ICV: This bit indicates the existence of ICV appended at the end of an encipherment packet.
1: No ICV appended
0: ICV appended</td></tr>
<tr><td>18:17</td><td>R/W</td><td>LBK1, LBK0</td><td>Loopback Test: There will be no packet on the TXI+/- and TXQ+/- lines under the Loopback test condition. The loopback function must be independent of the link state.
<table>
<tr><td>00: Normal operation</td><td>10: Baseband Loopback</td></tr>
<tr><td>01: MAC Loopback</td><td>11: Continue TX.</td></tr>
</table></td></tr>
<tr><td>16</td><td>R/W</td><td>CRC</td><td>Append CRC32: This bit indicates the existence of a CRC32 appended at the end of a packet.
1: No CRC32 appended
0: A CRC32 is appended</td></tr>
<tr><td>15:8</td><td>R/W</td><td>SRL</td><td>RTS Retry Limit: Indicates the maximum retry times of RTS frame, data or management frame of length less than or equal to RTSThreshold.</td></tr>
<tr><td>7:0</td><td>R/W</td><td>LRL</td><td>Data Packet Retry Limit: Indicates the maximum retransmission times of Data or Management frame of length greater than RTSThreshold.</td></tr>
</table>

6.8 RCR: Receive Configuration Register

(Offset 0044h-0047h, R/W)

This register is used to set the receive configuration for the RTL8180. Receive properties such as accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

Bit	R/W	Symbol	Description
31	R/W	ONLYERLPKT	**Early Receiving based on Packet Size:** Early Receiving is only performed for packets with a size greater than 1536 bytes.
30	R/W	ENCS2	**Enable Carrier Sense Detection Method 2**
29	R/W	ENCS1	**Enable Carrier Sense Detection Method 1**
28	R/W	ENMARP	**Enable MAC Autoreset PHY**
27:24	-	-	**Reserved**
23	R/W	CBSSID	**Check BSSID, To DS, From DS Match Packet:** When set to 1, the RTL8180 will check the Rx data type frame's BSSID, To DS and From DS fields, according to NETYPE (bits 3:2, MSR), to determine if it is set to Link ok at an Infrastructure or Adhoc network.
22	R/W	APWRMGT	**Accept Power Management Packet:** This bit will determine whether the RTL8180 will accept or reject packets with the power management bit set. 1: Accept 0: Reject
21	R/W	ADD3	**Accept Address 3 Match Packets:** Set this bit to 1 to accept broadcast/multicast data type frames that Address 3 matching RTL8180's MAC address. This bit is valid only when NETYPE (bits 3:2, MSR) is set to Link ok in an Infrastructure network.
20	R/W	AMF	**Accept Management Frame:** This bit will determine whether the RTL8180 will accept or reject a management frame. 1: Accept 0: Reject
19	R/W	ACF	**Accept Control Frame:** This bit will determine whether the RTL8180 will accept or reject a control frame. 1: Accept 0: Reject
18	R/W	ADF	**Accept Data Frame:** This bit will determine whether the RTL8180 will accept or reject a data frame. 1: Accept 0: Reject
17:16	-	-	**Reserved**
15:13	R/W	RXFTH2, 1, 0	**Rx FIFO Threshold:** This bit specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the Rx FIFO of the RTL8180, has reached to this level (or the FIFO has contained a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table:

000: Reserved	100: 256 bytes
001: Reserved	101: 512 bytes
010: 64 bytes	110: 1024 bytes
011:128 bytes	111: No Rx threshold. The RTL8180 begins the transfer of data after having received a whole packet into the FIFO.

Cont…

12	R/W	AICV	**Accept ICV Error Packet:** This bit determines whether all packets with ICV error will be accepted or rejected. 1: Accept 0: Reject
11	-	-	**Reserved**
10:8	R/W	MXDMA2, 1, 0	**Max DMA Burst Size per Rx DMA Burst:** This field sets the maximum size of the receive DMA data bursts according to the following table: 000: 16 bytes / 100: 256 bytes 001: 32 bytes / 101: 512 bytes 010: 64 bytes / 110: 1024 bytes 011: 128 bytes / 111: Unlimited
7	-	-	**Reserved**
6	R	9356SEL	**EEPROM Usage:** This bit reflects what type of EEPROM is used. 1: The EEPROM used is 9356 0: The EEPROM used is 9346
5	R/W	ACRC32	**Accept CRC32 Error Packet:** When set to 1, all packets with CRC32 error will be accepted. When set to 0, all packets with CRC32 error will be rejected. 1: Accept 0: Reject
4	-	-	**Reserved**
3	R/W	AB	**Accept Broadcast Packets:** This bit determines whether broadcast packets will be accepted or rejected. 1: Accept 0: Reject
2	R/W	AM	**Accept Multicast Packets:** This bit determines whether multicast packets will be accepted or rejected. 1: Accept 0: Reject
1	R/W	APM	**Accept Physical Match Packets:** This bit determines whether physical match packets will be accepted or rejected. 1: Accept 0: Reject
0	R/W	AAP	**Accept Destination Address Packets:** This bit determines whether all packets with a destination address will be accepted or rejected. 1: Accept 0: Reject

6.9 9346CR: 93C46 (93C56) Command Register (Offset 0050h, R/W)

This register is used for issuing commands to the RTL8180. These commands are issued by setting the corresponding bits for the function. A warm software reset along with individual reset and enable/disable for transmitter and receiver are provided as well.

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>EEM1-0</td><td>Operating Mode: These 2 bits select the RTL8180 operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal: The RTL8180 operates in network/host communication mode.</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load: Entering this mode will make the RTL8180 load the contents of the 93C46 (93C56) as when the RSTB signal is asserted. This auto-load operation will take about 2 ms. After it is completed, the RTL8180 will automatically return to normal mode (EEM1 = EEM0 = 0) and all the other registers are reset to default values.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 (93C56) Programming: In this mode, both network and host bus master operations are disabled. The 93C46 (93C56) can be directly accessed via bit3-0 which now reflects the states of the EECS, EESK, EEDI, and EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config Register Write Enable: Before writing to the CONFIG0, 1, 2, and 3 registers, the RTL8180 must be placed in this mode. This will prevent accidental change of the configurations of the RTL8180.</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>EECS</td><td rowspan="4">These bits reflect the state of the EECS, EESK, EEDI and EEDO pins in auto-load or 93C46 (93C56) programming mode.</td></tr>
<tr><td>2</td><td>R/W</td><td>EESK</td></tr>
<tr><td>1</td><td>R/W</td><td>EEDI</td></tr>
<tr><td>0</td><td>R</td><td>EEDO</td></tr>
</table>

6.10 CONFIG 0: Configuration Register 0 (Offset 0051h, R)

Bit	R/W	Symbol	Description
7	-	-	**Reserved**
6	R	WEP104	**104-Bit WEP Implemented:** Set to 1 to indicate that the optional 104-bit WEP scheme is implemented in the RTL8180. The initial value of this bit comes from the 93C46/ 93C56.
5	-	-	**Reserved**
4	R/W	LEDGPO_En	**LED Used as GPO Enable:** 1: Status of LED0-1 pins depends on the value of LEDGPO0-1 on Page Select Register (Offset 0x5E) 0: Status of LED0-1 pins follows the definition of 5.5 LED Interface.
3	R	Aux_Status	**Auxiliary Power Present Status:** This bit indicates the existence of Aux. power. The value of this bit is fixed after each PCI reset. 1: Aux. Power is present 0: Aux. Power is absent
2	-	-	**Reserved**
1:0	R	GL	**Geographic Location:** These bits indicate the current operational region in which RTL8180 transmits and receives packets. The initial value of these bits come from the 93C46/ 93C56.

Geographic Location	Bit 1	Bit 0
USA	1	1
Europe	1	0
Japan	0	1
Reserved	0	0

6.11 CONFIG 1: Configuration Register 1 (Offset 0052h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>LEDS1-0</td><td>Refer to the LED PIN definition. The initial value of these bits comes from the 93C46/93C56.</td></tr>
<tr><td>5</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>4</td><td>R/W</td><td>LWACT</td><td>LWAKE Active Mode: The LWACT bit and LWPTN bit in the CONFIG4 register are used to program the output signal of the LWAKE pin. According to the combination of these two bits, there are 4 choices for the LWAKE signal: Active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150 ms. In CardBus mode applications, LWACT and LWPTN bits have no meaning.

The default value of each of these two bits is 0, i.e., the default output signal of the LWAKE pin is an active high signal.
<table>
<tr><th colspan="2" rowspan="2">LWAKE Output</th><th colspan="2">LWACT</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td rowspan="2">LWPTN</td><td>0</td><td>Active high*</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
* Default value.</td></tr>
<tr><td>3</td><td>R</td><td>MEMMAP</td><td>Memory Mapping: The operational registers are mapped into PCI memory space.</td></tr>
<tr><td>2</td><td>R</td><td>IOMAP</td><td>I/O Mapping: The operational registers are mapped into PCI I/O space.</td></tr>
<tr><td>1</td><td>R/W</td><td>VPD</td><td>Vital Product Data: Set to enable Vital Product Data. The VPD data is stored in the 93C46 or 93C56 from within offset 40h-7Fh. If this bit is set, the New_Cap bit in the PCI Configuration Space (Offset 06h) of the RTL8180 is set, and the VPD registers are from offset 60h to 67h in the PCI Configuration Space of the RTL8180.</td></tr>
<tr><td>0</td><td>R/W</td><td>PMEn</td><td>Power Management Enable:
This bit is writable only when the 93C46CR register EEM1=EEM0=1.

Let A denote the New_Cap bit (bit 4 of the Status Register) in the PCI Configuration space offset 06h.
Let B denote the Cap_Ptr register in the PCI Configuration space offset 34h.
Let C denote the Cap_ID (power management) register in the PCI Configuration space offset 50h.
Let D denote the power management registers in the PCI Configuration space offset from 52h to 55h.
Let E denote the Next_Ptr (power management) register in the PCI Configuration space offset 51h.

PMEn Setting:
1: A=1, B=50h, C=01h, D is valid, E is valid and depends on whether or not VPD is enabled.
0: A=B=C=E=0, D is invalid. (Assume VPD bit = 0)</td></tr>
</table>

6.12 CONFIG 2: Configuration Register 2 (Offset 0053h, R/W)

Bit	R/W	Symbol	Description
7	R	LCK	**Locked Clocks:** Set this bit to 1 to indicate that the transmit frequency and symbol clocks are derived from the same oscillator. The initial value of this bit comes from the 93C46/93C56.
6	R	ANT	**Antenna Diversity:** The initial value of this bit comes from the 93C46/93C56. 1: Enable 0: Disable
5:4	-	-	**Reserved**
3	R/W	DPS	**Descriptor Polling State:** Test mode. This bit can not be auto-loaded from the EEPROM (9346 or 9356). See TPPoll (offset D9h). 0: Normal working state. This is also the power-on default value. 1: Test Mode
2	R/W	PAPE_sign	The initial value of this bit comes from the 93C46/93C56. 1: RTL8180 will advance PAPE_time to enable the PAPE pin when Tx data 0: RTL8180 will delay PAPE_time to enable the PAPE pin when Tx data
1:0	R/W	PAPE_time	These two bits indicate that the RTL8180 has enabled the PAPE pin in μs. The initial value of these bits come from the 93C46/93C56.

6.13 MSR: Media Status Register (Offset 0058h, R/W)

This register allows configuration of device and PHY options, and provides PHY status information.

Bit	R/W	Symbol	Description
7:4	-	-	**Reserved**
3:2	R/W	NETYPE	**Network Type and Link Status:** The values of these bits are written by the driver.
1:0	-	-	**Reserved**

Network Type	Bit 3	Bit 2
Reserved	1	1
Link ok at Infrastructure network	1	0
Link ok at Adhoc network	0	1
No Link	0	0

6.14 CONFIG 3: Configuration Register 3 (Offset 0059h, R/W)

Bit	R/W	Symbol	Description
7	R	GNTSel	**Grant Select:** This bit allows the selection of the Frame's asserted time after the Grant signal has been asserted. The Frame and Grant are the PCI signals. 0: No delay 1: Delay one clock from GNT assertion
6	R/W	PARM_En	**Parameter Write Enable:** Setting this bit to 1 and the 9346CR register EEM1=EEM0=1 enables the ANA_PARM register to be written via software.
5	R/W	Magic	**Magic Packet:** This bit is valid when the PMEn bit of the CONFIG1 register is set. The RTL8180 will assert the PMEB signal to wakeup the operating system when the Magic Packet is received. Once the RTL8180 has been enabled for Magic Packet wakeup and has been put into an adequate state, it scans all incoming packets addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame. A Magic Packet frame must also meet the basic requirements: Frame Control + Duration/ID + Destination address + Address 2 + Address 3 + Sequence Control + data + CRC The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of 6 byte ID registers, with no breaks or interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE address match the address of the ID registers. If the Node ID is 11h 22h 33h 44h 55h 66h, then the magic frame's format is like the following: Frame Control + Duration/ID + Destination address + Address 2 + Address 3 + Sequence Control + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4	-	-	**Reserved**
3	R	CardB_En	**Card Bus Enable:** 1: Enable CardBus related registers and functions 0: Disable CardBus related registers and functions
2	R	CLKRUN_En	**CLKRUN Enable:** 1: Enable CLKRUN 0: Disable CLKRUN
1	R	FuncRegEn	**Functions Registers Enable** (CardBus Only)**:** This bit enables the 4 Function Registers (Function Event Register, Function Event Mask Register, Function Present State Register, and Function Force Event Register) for CardBus applications. 1: Enable the 4 registers 2: Disable the 4 registers
0	R	FBtBEn	**Fast Back to Back Enable:** 1: Enable 0: Disable

6.15 CONFIG 4: Configuration Register 4 (Offset 005Ah, R/W)

Bit	R/W	Symbol	Description
7	R/W	VCOPDN	**VCO Power Down:** This bit can not be auto-loaded from the EEPROM (9346 or 9356). 1: VCO Power Down mode. Setting this bit will enable VCOPDN pin and turn off the external RF front end power (including VCO) and most of the internal power of the RTL8180. 0: Normal working state. This is the power-on default value.
6	R/W	PWROFF	**Power Off:** This bit can not be auto-loaded from the EEPROM (9346 or 9356). 1: Power Off mode. Turn off the external RF front end power (excluding VCO) and most of the internal power of the RTL8180. 0: Normal working state. This is the power-on default value.
5	R/W	PWRMGT	**Power Management:** This bit can not be auto-loaded from the EEPROM (9346 or 9356). 1: Power Management mode. Set Tx packet's power management bit to 1 include control type frame. 0: Normal working state. This is the power-on default value.
4	R/W	LWPME	**LANWAKE vs PMEB:** The initial value of this bit comes from the 93C46/ 93C56. In CardBus applications, this bit has no meaning. 1: LWAKE can only be asserted when PMEB is asserted and ISOLATEB is low. 0: LWAKE and PMEB are asserted at the same time.
3	-	-	**Reserved**
2	R/W	LWPTN	**LWAKE Pattern:** Please refer to the LWACT bit in the CONFIG1 register.
1:0	R/W	RFTYPE	**Radio Front End Programming Method:** The combination of these two bits indicate what kind of the RF module is being used with the RTL8180. The initial value of these bits comes from the 93C46/93C56.

RFE Type	Bit 1	Bit 0
Philips	1	1
RFMD	1	0
Intersil	0	1
Reserved	0	0

6.16 PSR: Page Select Register (Offset 005Eh, R/W)

Bit	R/W	Symbol	Description
7	R/W	GPO	**General Purpose Output:** This bit reflects and controls the status of pin52.
6	R	GPI	**General Purpose Input:** This bit reflects the status of pin64.
5	R/W	LEDGPO1	**LED1 Used as GPO:** When LEDGPO_En (Offset 0x51) is set to 1, this bit reflects and controls the status of LED1 pin.
4	R/W	LEDGPO0	**LED0 Used as GPO:** When LEDGPO_En (Offset 0x51) is set to 1, this bit reflects and controls the status of LED0 pin.
3:2	-	-	**Reserved**
1	R/W	UWF	**Unicast Wakeup Frame:** 1: Enable the Unicast Wakeup Frame with mask bytes of only the DID field, which is its own physical address. 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only the DID field, which is its own physical address.
0	R/W	PSEn	**Page Select Enable:** 1: Assign register 0084h-00D3h to be page 1. 0: Default value. Assign register 0084h-00D3h to be page 0.

6.17 SCR: Security Configuration Register (Offset 005Fh, R/W)

Bit	R/W	Symbol	Description
7:6	-	-	**Reserved**
5:4	R/W	KM	**Key Mode:** The combination of these two bits indicate what kind of security scheme is being used. Key Mode / Bit 5 / Bit 4 Reserved / 1 / 1 Reserved / 1 / 0 WEP104 / 0 / 1 WEP40 / 0 / 0
3:2	-	-	**Reserved**
1	R/W	TXSECON	**TX Security ON:** Set this bit to 1 to turn on the option security scheme of the Tx path. This bit is written by software and is invalid when WEP40 (bit 7, Config 0), and WEP104 (bit 6, Config 0) are set to 0.
0	R/W	RXSECON	**RX Security ON:** Set this bit to 1 to turn on the option security scheme of the Rx path. This bit is written by software and is invalid when WEP40 (bit 7, Config 0), and WEP104 (bit 6, Config 0) are set to 0.

6.18 BcnItv: Beacon Interval Register (Offset 0070h-0071h, R/W)

Bit	R/W	Symbol	Description
15:10	-	-	**Reserved**
9:0	R/W	BcnItv	**Beacon Interval:** The Beacon Interval represents the number of time units (1 TU = 1024μs) between target beacon transmission times (TBTTs). This register is written by the driver after the NIC joins a network or creates an adhoc network.

6.19 AtimWnd: Atim Window Register (Offset 0072h-0073h, R/W)

Bit	R/W	Symbol	Description
15:10	-	-	**Reserved**
9:0	R/W	AtimWnd	This register indicates the ATIM Window length in TU. It is written by the driver after the NIC joins or creates an adhoc network.

6.20 BintrItv: Beacon Interrupt Interval Register (Offset 0074h-0075h, R/W)

Bit	R/W	Symbol	Description
15:10	-	-	**Reserved**
9:0	R/W	BintrItv	This timer register will generate BcnInt (bit 13, ISR) at a setting time interval before TBTT to prompt the host to prepare the beacon. The units of this register is microseconds. It is written by the driver after the NIC joins a network or creates an adhoc network.

6.21 AtimtrItv: Atim Interrupt Interval Register (Offset 0076h-0077h, R/W)

Bit	R/W	Symbol	Description
15:10	-	-	**Reserved**
9:0	R/W	AtimtrItv	This timer register will generate ATIMInt (bit 12, ISR) at a setting time interval before the end of the ATIM window in an adhoc network. The units of this register is microseconds. It is written by the driver after the NIC joins a network or creates an adhoc network.

6.22 PhyDelay: Phy Delay Register (Offset 0078h, R/W)

Bit	R/W	Symbol	Description
7:3	-	-	**Reserved**
2:0	R/W	PhyDelay	**Physical Layer Delay Time:** These three bits represent the delay time in μs between the MAC and RF front end when Tx data.

6.23 DK0: Default Key 0 Register (Offset 0090h-009Fh, R/W)

Bit	R/W	Symbol	Description
127:104	-	-	**Reserved**
103:0	R/W	DK0	**Default Key 0:** These 104 bits (bits 103:0) indicate the default 104-bit WEP key, which the ID is 0 when KM (bits 5:4, SCR) is set to WEP104, the 24 most significant bits (bits 127:103) will be reserved. The 40 least significant bits (bits 39:0) indicate the default 40-bit WEP key, which the ID is 0 when KM is set to WEP40, and the 64 most significant bits (bits 103:40) will be reserved. This register is only permitted to read/write by 4-byte access.

6.24 DK1: Default Key 1 Register (Offset 00A0h-00AFh, R/W)

Bit	R/W	Symbol	Description
127:104	-	-	**Reserved**
103:0	R/W	DK1	**Default Key 1:** These 104 bits (bits 103:0) indicate the default 104-bit WEP key, which the ID is 1 when KM (bits 5:4, SCR) is set to WEP104, the 24 most significant bits (bits 127:103) will be reserved. The 40 least significant bits (bits 39:0) indicate the default 40-bit WEP key, which the ID is 1 when KM is set to WEP40, and the 64 most significant bits (bits 103:40) will be reserved. This register is only permitted to read/write by 4-byte access.

6.25 DK2: Default Key 2 Register (Offset 00B0h-00BFh, R/W)

Bit	R/W	Symbol	Description
127:104	-	-	**Reserved**
103:0	R/W	DK2	**Default Key 2:** These 104 bits (bits 103:0) indicate the default 104-bit WEP key, which the ID is 2 when KM (bits 5:4, SCR) is set to WEP104, the 24 most significant bits (bits 127:103) will be reserved. The 40 least significant bits (bits 39:0) indicate the default 40-bit WEP key, which the ID is 2 when KM is set to WEP40, and the 64 most significant bits (bits 103:40) will be reserved. This register is only permitted to read/write by 4-byte access.

6.26 DK3: Default Key 3 Register

(Offset 00C0h-00CFh, R/W)

Bit	R/W	Symbol	Description
127:104	-	-	**Reserved**
103:0	R/W	DK3	**Default Key 3:** These 104 bits (bits 103:0) indicate the default 104-bit WEP key, which the ID is 3 when KM (bits 5:4, SCR) is set to WEP104, the 24 most significant bits (bits 127:103) will be reserved. The 40 least significant bits (bits 39:0) indicate the default 40-bit WEP key, which the ID is 3 when KM is set to WEP40, and the 64 most significant bits (bits 103:40) will be reserved. This register is only permitted to read/write by 4-byte access.

6.27 CONFIG 5: Configuration Register 5

(Offset 00D8h, R/W)

This register, unlike other Configuration registers, is not protected by the 93C46 Command register. Therefore, there is no need to enable the Config register write prior to writing to Config5.

Bit	R/W	Symbol	Description
7	R	TX_FIFO_OK	**Built in Self Test for TX FIFO:** 1: OK 0: Fail
6	R	RX_FIFO_OK	**Built in Self Test for RX FIFO:** 1: OK 0: Fail
5	R/W	CALON	**Calibration ON:** This bit can not be auto-loaded from the EEPROM (9346 or 9356). 1: Activate the calibration cycle, and hold AGCRESET pin to high 0: Put AGCRESET pin to ground
4:3	-	-	**Reserved**
2	R/W	EACPI	**Enable ACPI Wake up:** This bit can not be auto-loaded from the EEPROM (9346 or 9356). 1: Enable ACPI Wake On LAN 0: Default value. Disable ACPI WOL
1	R/W	LANWake	**LANWake Signal Enable/Disable:** This bit initial value comes from the 93C46/ 93C56. 1: Enable LANWake signal 0: Disable LANWake signal
0	R/W	PME_STS	**PME_Status Bit:** Always sticky/can be reset by PCI RST# and software. The initial value of this bit comes from the 93C46/ 93C56. 1: The PME_Status bit can be reset by a PCI reset or by software. 0: The PME_Status bit can only be reset by software.

6.28 TPPoll: Transmit Priority Polling Register (Offset 00D9h, W)

Bit	R/W	Symbol	Description
7	W	BQ	**Beacon Queue Polling:** i. The RTL8180 will clear this bit automatically after a beacon packet has been transmitted or received. ii. Writing to this bit has no effect.
6	W	HPQ	**High Priority Queue Polling:** i. Write a 1 to this bit by software to notify the RTL8180 that there is a high priority packet(s) waiting to be transmitted. ii. The RTL8180 will clear this bit automatically after all high priority packets have been transmitted. iii. Writing a 0 to this bit has no effect.
5	W	NPQ	**Normal Priority Queue Polling:** DPS (bit3, Config 2) set to 0: i. The RTL8180 will clear this bit automatically after all normal priority packets have been transmitted or received. ii. Writing to this bit has no effect. DPS (bit3, Config 2) set to 1: i. Write a 1 to this bit by software to notify the RTL8180 that there is a normal priority packet(s) waiting to be transmitted. ii. The RTL8180 will clear this bit automatically after all normal priority packets have been transmitted. iii. Writing a 0 to this bit has no effect.
4	W	LPQ	**Low Priority Queue Polling:** i. Write a 1 to this bit by software to notify the RTL8180 that there is a low priority packet(s) waiting to be transmitted. ii. The RTL8180 will clear this bit automatically after all low priority packets have been transmitted. iii. Writing a 0 to this bit has no effect.
3	W	SBQ	**Stop Beacon Queue:** Write a 1 to this bit by software to notify the RTL8180 to stop the DMA mechanism of the Beacon Queue. This bit is invalid when DPS (bit3, Config 2) is set to 1.
2	W	SHPQ	**Stop High Priority Queue:** Write a 1 to this bit by software to notify the RTL8180 to stop the DMA mechanism of the High Priority Queue.
1	W	SNPQ	**Stop Normal Priority Queue:** Write a 1 to this bit by software to notify the RTL8180 to stop the DMA mechanism of the Normal Priority Queue. This bit is invalid when DPS (bit3, Config 2) is set to 1.
0	W	SLPQ	**Stop Low Priority Queue:** Write a 1 to this bit by software to notify the RTL8180 to stop the DMA mechanism of the Low Priority Queue.

6.29 CWR: Contention Window Register (Offset 00DCh-00DDh, R)

Bit	R/W	Symbol	Description
15:10	-	-	**Reserved**
9:0	R	CW	**Contention Window:** This register indicates the number of contention windows before transmitting a packet.

6.30 RetryCTR: Retry Count Register (Offset 00DEh, R)

Bit	R/W	Symbol	Description
7:0	R	RetryCT	**Retry Count:** This register indicates the number of retry counts when a packet transmit is completed.

6.31 RDSAR: Receive Descriptor Start Address Register (Offset 00E4h-00E7h, R/W)

Bit	R/W	Symbol	Description
31:0	R/W	RDSA	**Receive Descriptor Start Address:** This is a 32-bit address.

6.32 FER: Function Event Register (Offset 00F0h-00F3h, R/W)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	R/W	INTR	**Interrupt:** This bit is set to 1 when INTR field in the Function Force Event Register is set. Writing a 1 may clear this bit. Writing a 0 has no effect. This bit must not be affected by RST# pin and software reset.
14:5	-	-	**Reserved**
4	R/W	GWAKE	General Wakeup: This bit is set to 1 when the GWAKE field in the Function Present State Register changes its state from 0 to 1. This bit can also be set when the GWAKE bit of the Function Force Register is set. Writing a 1 may clear this bit. Writing a 0 has no effect. This bit can not be affected by the RST# pin.
3:0	-	-	**Reserved**

- Ø This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).
- Ø The Function Event (Offset F0h), Function Event Mask (Offset F4h), Function Present State (Offset F8h), and Function Force Event (Offset FCh) registers have some corresponding fields with the same names. The GWAKE and INTR bits of these registers reflect the wake-up event signaled on the SCTCSCHG pin. The operation of the CSTCSCHG pin is similar to the PME# pin except that the CSTCSCHG pin is asserted high.

6.33 FEMR: Function Event Mask Register (Offset 00F4h-00F7h, R/W)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	R/W	INTR	**Interrupt Mask:** When cleared (0), setting of the INTR bit in either the Function Present State Register or the Function Event Register will not cause assertion of the INT# signal while the CardBus PC Card interface is powered up, or the system Wakeup (CSTSCHG) while the interface is powered off. Setting this bit to 1 enables the INTR bit in both the Function Present State Register and the Function Event Register to generate the INT# signal. It also enables the system Wakeup if the corresponding WKUP field in this Function Event Mask Register is also set. This bit is not affected by RST#.
14	R/W	WKUP	**Wakeup Mask:** When cleared (0), the Wakeup function is disabled, i.e., the setting of this bit in the Function Event Register will not assert the CSTSCHG signal. Setting this bit to 1 enables the fields in the Function Event Register to assert the CSTSCHG signal. This bit is not affected by RST#.
13:5	-	-	**Reserved**
4	R/W	GWAKE	**General Wakeup Mask:** When cleared (0), setting this bit in the Function Event Register will not cause the assertion of the CSTSCHG pin. Setting this bit to 1, enables the GWAKE field in the Function Event Register to assert the CSTSCHG pin if bit14 of this register is also set. This bit is not affected by RST#.
3:0	-	-	**Reserved**

- Ø This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).

6.34 FPSR: Function Present State Register (Offset 00F8h-00FBh, R)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	R	INTR	**Interrupt:** This bit is set when one of the ISR register bits has been set to 1. It remains set (1), until all of the ISR register bits have been cleared. This bit is not affected by RST#.
14:5	-	-	**Reserved**
4	R	GWAKE	**General Wakeup:** This bit reflects the current state of the Wakeup event(s), and is similar to the PME_Status bit of the PMCSR register. It remains set (1), until the PME_Status bit of the PMCSR register is cleared. This bit is not affected by RST#.
3:0	-	-	**Reserved**

- Ø This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).
- Ø This read-only register reflects the current state of the function.

6.35 FFER: Function Force Event Register

(Offset 00FCh-00FFh, W)

Bit	R/W	Symbol	Description
31:16	-	-	**Reserved**
15	W	INTR	**Interrupt:** Writing a 1 to this bit sets the INTR bit in the Function Event Register. However, the INTR bit in the Function Present State Register is not affected and continues to reflect the current state of the ISR register. Writing a 0 to this bit has no effect.
14:5	-	-	**Reserved**
4	W	GWAKE	**General Wakeup:** Setting this bit to 1 sets the GWAKE bit in the Function Event Register. However, the GWAKE bit in the Function Present State Register is not affected and continues to reflect the current state of the Wakeup request. Writing a 0 to this bit has no effect.
3:0	-	-	**Reserved**

Ø This register is valid only when Card_En=1 (bit3, Config3) and FuncRegEn=1 (bit1, Config3).

7. EEPROM (93C46 or 93C56) Contents

The RTL8180 supports the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM). The EEPROM interface provides the ability for the RTL8180 to read from and write data to an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following internal power on reset or software EEPROM autoload command. The RTL8180 will autoload values from the EEPROM to these fields in configuration space and I/O space. If the EEPROM is not present, the RTL8180 initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using "bit-bang" accesses via the 9346CR Register.

Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the initial power on or auto-load command in 9346CR, the RTL8180 performs a series of EEPROM read operations from the 93C46 (93C56) addresses 00h to 31h.

- It is suggested to obtain Realtek approval before changing the default settings of the EEPROM.

Bytes	Contents	Description
00h 01h	29h 81h	These 2 bytes contain the ID code word for the RTL8180. The RTL8180 will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct otherwise, the Vendor ID and Device ID of the PCI configuration space are "10ECh" and "8180h".
02h-03h	VID	**PCI Vendor ID:** PCI configuration space offset 00h-01h.
04h-05h	DID	**PCI Device ID:** PCI configuration space offset 02h-03h.
06h-07h	SVID	**PCI Subsystem Vendor ID:** PCI configuration space offset 2Ch-2Dh.
08h-09h	SMID	**PCI Subsystem ID:** PCI configuration space offset 2Eh-2Fh.
0Ah	MNGNT	**PCI Minimum Grant Timer:** PCI configuration space offset 3Eh.
0Bh	MXLAT	**PCI Maximum Latency Timer:** PCI configuration space offset 3Fh.
0Ch	RFChipID	**RF chip identifier.**
0Dh	CONFIG3	**RTL8180 Configuration register 3:** operational register offset 59h.
0Eh-13h	MAC Address	**MAC Address:** After the auto-load command or a hardware reset, the RTL8180 loads MAC Addresses to IDR0-IDR5 of the I/O registers of the RTL8180.
14h	CONFIG0	**RTL8180 Configuration register 0:** Operational register offset 51h.
15h	CONFIG1	**RTL8180 Configuration register 1:** Operational register offset 52h.
16h-17h	PMC	**Reserved:** Do not change this filed without Realtek approval. **Power Management Capabilities:** PCI configuration space address 52h and 53h.
18h	CONFIG2	**RTL8180 Configuration register 2:** Operational register offset 53h.
19h	CONFIG4	**RTL8180 Configuration register 4:** Operational register offset 5Ah.
1Ah-1Dh	ANA_PARM	**Reserved:** Do not change this filed without Realtek approval. **Analog Parameter for the RTL8180:** Operational registers of the RTL8180 are from 54h to 57h.
1Eh	TESTR	**Reserved:** Do not change this filed without Realtek approval. **RTL8180 Test Mode Register:** Operational register offset 5Bh.
1Fh	CONFIG5	**RTL8180 Configuration register 5:** Operational register offset D8h. Do not change this filed without Realtek approval. Bit7:2: Reserved. Bit1: LANWake signal Enable/Disable 1: Enable LANWake signal. 0: Disable LANWake signal. Bit0: PME_Status bit property 1: The PME_Status bit can be reset by PCI reset or by software if D3cold_support_PME is 0. If D3cold_support_PME=1, the PME_Status bit is a sticky bit. 0: The PME_Status bit is always a sticky bit and can only be reset by software.

Cont…

20h	TxPower1	**Transmit Power Level for 802.11b-defined channel_ID 1** (center frequency=2412MHz)
21h	TxPower2	**Transmit Power Level for 802.11b-defined channel_ID 2** (center frequency=2417MHz)
22h	TxPower3	**Transmit Power Level for 802.11b-defined channel_ID 3** (center frequency=2422MHz)
23h	TxPower4	**Transmit Power Level for 802.11b-defined channel_ID 4** (center frequency=2427MHz)
24h	TxPower5	**Transmit Power Level for 802.11b-defined channel_ID 5** (center frequency=2432MHz)
25h	TxPower6	**Transmit Power Level for 802.11b-defined channel_ID 6** (center frequency=2437MHz)
26h	TxPower7	**Transmit Power Level for 802.11b-defined channel_ID 7** (center frequency=2442MHz)
27h	TxPower8	**Transmit Power Level for 802.11b-defined channel_ID 8** (center frequency=2447MHz)
28h	TxPower9	**Transmit Power Level for 802.11b-defined channel_ID 9** (center frequency=2452MHz)
29h	TxPower10	**Transmit Power Level for 802.11b-defined channel_ID 10** (center frequency=2457MHz)
2Ah	TxPower11	**Transmit Power Level for 802.11b-defined channel_ID 11** (center frequency=2462MHz)
2Bh	TxPower12	**Transmit Power Level for 802.11b-defined channel_ID 12** (center frequency=2467MHz)
2Ch	TxPower13	**Transmit Power Level for 802.11b-defined channel_ID 13** (center frequency=2472MHz)
2Dh	TxPower14	**Transmit Power Level for 802.11b-defined channel_ID 14** (center frequency=2484MHz)
2Eh	ChannelPlan	**Map of channels to be scanned.**
2Fh	EnergyDetThr	**Energy detect threshold.**
30h-31h	CISPointer	**Reserved:** Do not change this filed without Realtek approval. **CIS Pointer**
32h	RFParm	**RF specific parameter**
33h-3Bh	-	**Reserved**
3Ch-3Dh	Version	**Version information of EEPROM content.**
3Eh-3Fh	CRC	**16bit CRC value of EEPROM content.**
40h-7Fh	VPD_Data	**VPD Data Field:** Offset 40h is the start address of the VPD data.
80h-FFh	CIS_Data	**CIS Data Field:** Offset 80h is the start address of the CIS data. (93C56 only).

7.1 Summary of RTL8180 EEPROM Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	R/W*								
51h	CONFIG0	R	WEP40	WEP104	-	-	-	-	GL	
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	-	LWACT	MEMMAP	IOMAP	VPD	PMEN
		W*	LEDS1	LEDS0	-	LWACT	-	-	VPD	PMEN
53h	CONFIG2	R	LCK	ANT	-	-	-	PAPE_sign	PAPE_time	
		W*	-	-	-	-	-	PAPE_sign	PAPE_time	
54h-57h	ANA_PARM	R/W**	32-bit Read Write							
59h	CONFIG3	R	GNTSel	PARM_En	Magic	-	CardB_En	CLKRUN_En	FuncRegEn	FBtBEn
		W*	-	PARM_En	Magic	-	-	-	-	-
5Ah	CONFIG4	R	-	-	-	LWPME	-	LWPTN	RFTYPE	
		W*	-	-	-	LWPME	-	LWPTN	-	
5Bh	TESTR	R/W	8-bit Read Write							
D8h	CONFIG5	R/W*	-	-	-	-	-	-	LANWake	PME_STS

* The registers marked with type = 'W*' can be written only if bits EEM1=EEM0=1.

7.2 Summary of EEPROM Power Management Registers

Configuration Space Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

8. PCI Configuration Space Registers

8.1 PCI Bus Interface

The RTL8180 implements the PCI bus interface as defined in the PCI Local Bus Specifications Rev. 2.2. When internal registers are being accessed, the RTL8180 acts as a PCI target (slave mode). When accessing host memory for descriptor or packet data transfer, the RTL8180 acts as a PCI bus master.

All of the required pins and functions are implemented in the RTL8180 as well as the optional pin, INTAB for support of interrupt requests is implemented as well. For more information, refer to the PCI Local Bus Specifications Rev. 2.2, December 18, 1998.

8.1.1 Interrupt Control

Interrupts are performed by asynchronously asserting the INTAB pin. This pin is an open drain output. The source of the interrupt can be determined by reading the Interrupt Status Register (ISR). One or more bits in the ISR will be set, denoting all currently pending interrupts. Reading of the ISR clears all bits. Masking of specific interrupts can be accomplished by using the Interrupt Mask Register (IMR). Assertion of INTAB can be prevented by clearing the Interrupt Enable bit in the Interrupt Mask Register. This allows the system to defer interrupt processing as needed.

8.1.2 Latency Timer

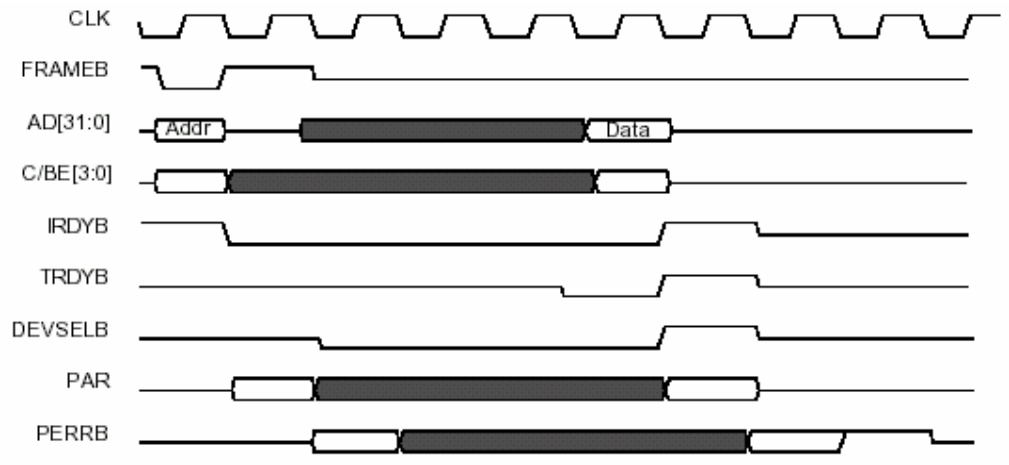
The PCI Latency Timer described in MXLAT defines the maximum number of bus clocks that the device will hold the bus. Once the device gains control of the bus and issues FRAMEB, the Latency Timer will begin counting down. If GNTB is deasserted before the RTL8180 has finished with the bus, the device will maintain ownership of the bus until the timer reaches zero (or has finished the bus transfer). This means that the timer value can only be incremented in units of 16 clocks.

8.2 Bus Operation

8.2.1 Target Read

A Target Read operation starts with the system generating FRAMEB, Address, and either an IO read (0010b) or Memory Read (0110b) command. If the 32-bit address on the address bus matches the IO address range specified in IOAR (for I/O reads) or the memory address range specified in MEM (for memory reads), the RTL8180 will generate DEVSELB 2 clock cycles later (medium speed). The system must tri-state the Address bus, and convert the C/BE bus to byte enables, after the address cycle. On the 2nd cycle after the assertion of DEVSELB, all 32-bits of data and TRDYB will become valid. If IRDYB is asserted at that time, TRDYB will be forced HIGH on the next clock for 1 cycle, and then tri-stated.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8180 will still make data available as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.

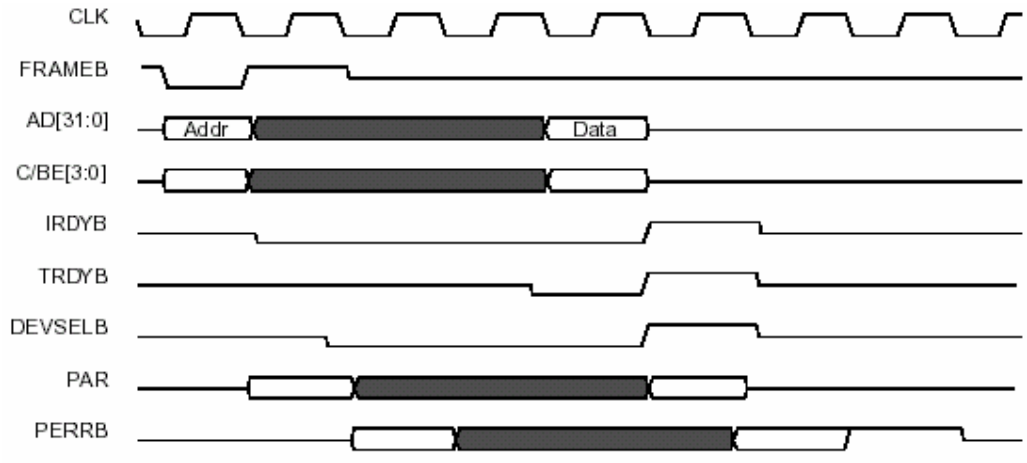


Target Read Operation

8.2.2 Target Write

A Target Write operation starts with the system generating FRAMEB, Address, and Command (0011b or 0111b). If the upper 24 bits on the address bus match IOAR (for I/O reads) or MEM (for memory reads), the RTL8180 will generate DEVSELB 2 clock cycles later. On the 2nd cycle after the assertion of DEVSELB, the device will monitor the IRDYB signal. If IRDYB is asserted at that time, the RTL8180 will assert TRDYB. On the next clock the 32-bit double word will be latched in, and TRDYB will be forced HIGH for 1 cycle and then tri-stated. Target write operations must be 32-bits wide.

If FRAMEB is asserted beyond the assertion of IRDYB, the RTL8180 will still latch the first double word as described above, but will also issue a Disconnect. That is, it will assert the STOPB signal with TRDYB. STOPB will remain asserted until FRAMEB is detected as deasserted.



Target Write Operation

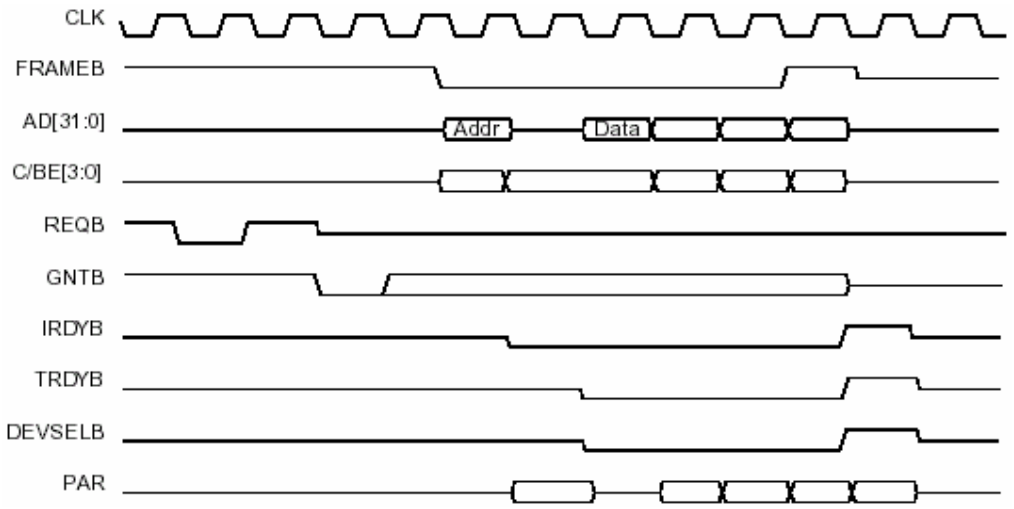
8.2.3 Master Read

A Master Read operation starts with the RTL8180 asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a master abort by asserting FRAMEB HIGH for 1 cycle, and IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the address bus will become tri-state, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, data will be latched in (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last read cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the read operation. The RTL8180 will never force a wait state during a read operation.



Master Read Operation

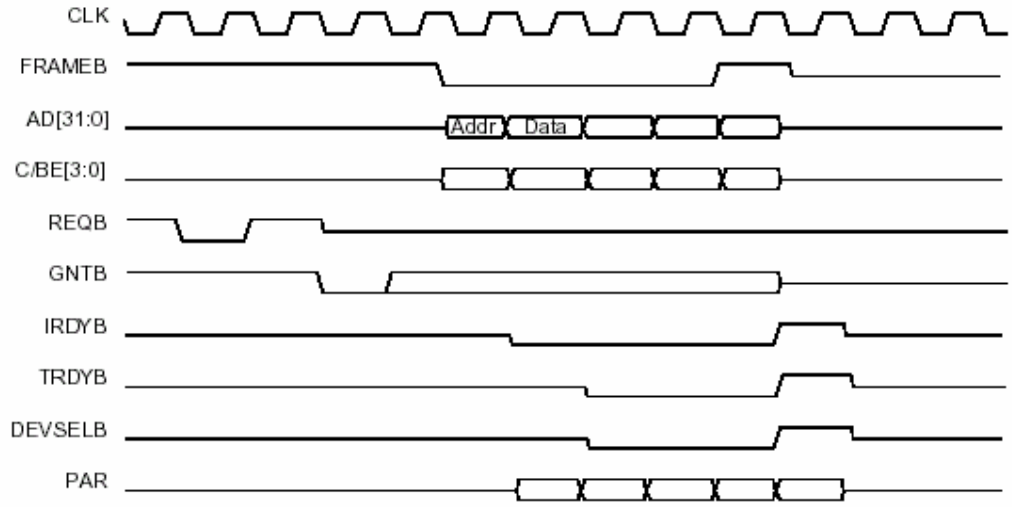
8.2.4 Master Write

A Master Write operation starts with the RTL8180 asserting REQB. If GNTB is asserted within 2 clock cycles, FRAMEB, Address, and Command will be generated 2 clocks after REQB (Address and FRAMEB for 1 cycle only). If GNTB is asserted 3 cycles or later, FRAMEB, Address, and Command will be generated on the clock following GNTB.

The device will wait for 8 cycles for the assertion of DEVSELB. If DEVSELB is not asserted within 8 clocks, the device will issue a Master Abort by asserting FRAMEB HIGH for 1 cycle. IRDYB will be forced HIGH on the following cycle. Both signals will become tri-state on the cycle following their deassertion.

On the clock edge after the generation of Address and Command, the data bus will become valid, and the C/BE bus will contain valid byte enables. On the clock edge after FRAMEB was asserted, IRDYB will be asserted (and FRAMEB will be deasserted if this is to be a single read operation). On the clock where both TRDYB and DEVSELB are detected as asserted, valid data for the next cycle will become available (and the byte enables will change if necessary). This will continue until the cycle following the deassertion of FRAMEB.

On the clock where the second to last write cycle occurs, FRAMEB will be forced HIGH (it will be tri-stated 1 cycle later). On the next clock edge that the device detects TRDYB asserted, it will force IRDYB HIGH. It, too, will be tri-stated 1 cycle later. This will conclude the write operation. The RTL8180 will never force a wait state during a write operation.



Master Write Operation

8.2.5 Configuration Access

Configuration register accesses are similar to target reads and writes in that they are single data word transfers and are initiated by the system. For the system to initiate a Configuration access, it must also generate IDSEL as well as the correct Command (1010b or 1011b) during the Address phase. The RTL8180 will respond as it does during Target operations. Configuration reads must be 32-bits wide, but writes may access individual bytes.

8.3 Packet Buffering

The RTL8180 incorporates two independent FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data freeing the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the Receive Configuration registers. These values determine how full or empty the FIFOs must be before the device requests the bus. Once the RTL8180 requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in the Transmit Configuration and Receive Configuration registers.

8.3.1 Transmit Buffer Manager

The buffer management scheme used on the RTL8180 allows quick, simple and efficient use of the frame buffer memory. The buffer management scheme uses separate buffers and descriptors for packet information. This allows effective transfers of data to the transmit buffer manager by simply transferring the descriptor information to the transmit queue.

The Tx Buffer Manager DMAs packet data from system memory and places it in the 4KB transmit FIFO, and pulls data from the FIFO to send to the Tx MAC. Multiple packets may be present in the FIFO, allowing packets to be transmitted with short interframe space. Additionally, once the RTL8180 requests the bus, it will attempt to fill the FIFO as allowed by the MXDMA setting.

The Tx Buffer Manager process also supports priority queuing of transmit packets. It handles this by drawing from two separate descriptor lists to fill the internal FIFO. If packets are available in the high priority queues, they will be loaded into the FIFO before those of low priority.

8.3.2 Receive Buffer Manager

The Rx Buffer Manager uses the same buffer management scheme as used for transmits. The Rx Buffer Manager retrieves packet data from the Rx MAC and places it in the 2KB receive data FIFO, and pulls data from the FIFO for DMA to system memory. The receive FIFO is controlled by the FIFO threshold value in RXFTH. This value determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory occurs. Once the RTL8180 gets the bus, it will continue to transfer the long words from the FIFO until the data in the FIFO is less than one long word, or has reached the end of the packet, or the max DMA burst size is reached, as set in MXDMA.

8.3.3 Packet Recognition

The Rx packet filter and recognition logic allows software to control which packets are accepted, based on destination address and packet type. Address recognition logic includes support for broadcast, multicast hash, and unicast addresses. The packet recognition logic includes support for WOL and programmable pattern recognition.

8.4 PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	MWIEN	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	FBTBEN	SERREN
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	FBBC	0	0	NewCap	0	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	DST1	DST0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R/W	0	0	0	0	0	0	0	0
0Dh	LTR	R	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		R/W	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		R/W	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		R/W	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h	MEMAR	R	0	0	0	0	0	0	0	MEMIN
		W	-	-	-	-	-	-	-	-
15h		R/W	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
16h		R/W	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
17h		R/W	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
18h-27h	RESERVED									
28h-2Bh	CISPtr	Cardbus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	1	0	0	0	0
35h-3Bh	RESERVED									

Cont…

3Ch	ILR	R/W	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h-4Fh	RESERVED									
50h	PMID	R	0	0	0	0	0	0	0	1
51h	NextPtr	R	0	0	0	0	0	0	0	0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
54h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
55h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
56h-5Fh	RESERVED									
60h	VPDID	R	0	0	0	0	0	0	1	1
61h	NextPtr	R	0	0	0	0	0	0	0	0
62h	Flag VPD Address	R/W	VPDADDR7	VPDADDR6	VPDADDR5	VPDADDR4	VPDADDR3	VPDADDR2	VPDADDR1	VPDADDR0
63h		R/W	Flag	VPDADDR14	VPDADDR13	VPDADDR12	VPDADDR11	VPDADDR10	VPDADDR9	VPDADDR8
64h	VPD Data	R/W	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
65h		R/W	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
66h		R/W	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
67h		R/W	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
68h-FFh	RESERVED									

[2] The above table is based on a status with both VPD and Power Management enabled.

8.5 PCI Configuration Space Functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the configuration space of the RTL8180 are described below.

VID: Vendor ID. This field will be set to a value corresponding to PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh, which is Realtek Semiconductor's PCI Vendor ID.

DID: Device ID. This field will be set to a value corresponding to PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8180h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Symbol	Description
15:10	-	**Reserved**
9	FBTBEN	**Fast Back-To-Back Enable:** Config2<FBtBEn>=0: Read as 0. Write operation has no effect. The RTL8180 will not generate Fast Back-to-back cycles. When Config2<FbtBEn>=1, this read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 indicates the master is allowed to generate fast back-to-back transaction to different agents. A value of 0 indicates fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0.
8	SERREN	**System Error Enable:** When set to 1, the RTL8180 asserts the SERRB pin when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0>).
7	ADSTEP	**Address/Data Stepping:** Read as 0, write operation has no effect. The RTL8180 will not generate address/data stepping.
6	PERRSP	**Parity Error Response:** When set to 1, the RTL8180 will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When set to 0, any detected parity error is ignored and the RTL8180 continues normal operation. Parity checking is disabled after hardware reset (RSTB).
5	VGASNOOP	**VGA Palette SNOOP:** Read as 0, write operation has no effect.
4	MWIEN	**Memory Write and Invalidate Cycle Enable:** This is an enable bit for using the Memory Write and Invalidate commands. When this bit is 1, the RTL8180 as a master may generate the command. When this bit is 0, the RTL8180 may generate a Memory Write command instead. State after PCI RSTB is 0.
3	SCYCEN	**Special Cycle Enable:** Read as 0, write operation has no effect. The RTL8180 ignores all special cycle operations.
2	BMEN	**Bus Master Enable:** When set to 1, the RTL8180 is capable of acting as a bus master. When set to 0, it is prohibited from acting as a PCI bus master. For normal operation, this bit must be set by the system BIOS.
1	MEMEN	**Memory Space Access:** When set to 1, the RTL8180 responds to memory space accesses. When set to 0, the RTL8180 ignores memory space accesses.
0	IOEN	**I/O Space Access:** When set to 1, the RTL8180 responds to IO space access. When set to 0, the RTL8180 ignores I/O space accesses.

Status: The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit	Symbol	Description
15	DPERR	**Detected Parity Error:** When this bit is set, it indicates that the RTL8180 has detected a parity error, even if parity error handling is disabled in the command register PERRSP bit.
14	SSERR	**Signaled System Error:** When this bit is set, it indicates that the RTL8180 has asserted the system error pin, SERRB. Writing a 1 clears this bit to 0.
13	RMABT	**Received Master Abort:** When this bit is set, it indicates that the RTL8180 has terminated a master transaction with a master abort. Writing a 1 clears this bit to 0.
12	RTABT	**Received Target Abort:** When this bit is set, it indicates that the RTL8180 master transaction was terminated due to a target abort. Writing a 1 clears this bit to 0.
11	STABT	**Signaled Target Abort:** This bit is set to 1 whenever the RTL8180 terminates a transaction with a target abort. Writing a 1 clears this bit to 0.
10:9	DST1-0	**Device Select Timing:** These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8180 will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	**Data Parity error Detected:** This bit sets when the following conditions are met: • The RTL8180 asserts parity error (PERRB pin) or it senses the assertion of the PERRB pin by another device. • The RTL8180 operates as a bus master for the operation that caused the error. • The Command register PERRSP bit is set. Writing a 1 clears this bit to 0.
7	FBBC	**Fast Back-To-Back Capable:** Config2<FBtBEn>=0, Read as 0, write operation has no effect. Config2<FBtBEn>=1, Read as 1.
6	UDF	**User Definable Features Supported:** Read as 0, write operation has no effect. The RTL8180 does not support UDF.
5	66MHz	**66 MHz Capable:** Read as 0, write operation has no effect. The RTL8180 has no 66MHz capability.
4	NewCap	**New Capability:** Config1<PMEn>=0, Read as 0, write operation has no effect. Config1<PMEn>=1, Read as 1.
0:3	-	**Reserved**

RID: Revision ID Register

The Revision ID register is an 8-bit register that specifies the RTL8180 controller revision number.

PIFR: Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8180 controller. The PCI specification reversion 2.1 doesn't define any other specific value for network devices. So PIFR = 00h.

SCR: Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the RTL8180. SCR = 00h indicates that the RTL8180 is an Ethernet controller.

BCR: Base-Class Register

The Base-class register is an 8-bit register that broadly classifies the function of the RTL8180. BCR = 02h indicates that the RTL8180 is a network controller.

CLS: Cache Line Size

Specifies, in units of 32-bit words (double-words), the system cache line size. The RTL8180 supports cache line size of 8, and 16 longwords (DWORDs). The RTL8180 uses Cache Line Size for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple, and memory-write-and-invalidate.

LTR: Latency Timer Register

Specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8180.

When the RTL8180 asserts FRAMEB, it enables its latency timer to count. If the RTL8180 deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the RTL8180 initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00h.

HTR: Header Type Register

Reads will return a 0, writes are ignored.

BIST: Built-in Self Test

Reads will return a 0, writes are ignored.

IOAR: This register specifies the BASE IO address, which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

Bit	Symbol	Description
31:8	IOAR31-8	**BASE IO Address:** This is set by software to the Base IO address for the operational register map.
7:2	IOSIZE	**Size Indication:** Read back as 0. This allows the PCI bridge to determine that the RTL8180 requires 256 bytes of IO space.
1	-	**Reserved**
0	IOIN	**IO Space Indicator:** Read only. Set to 1 by the RTL8180 to indicate that it is capable of being mapped into IO space.

MEMAR: This register specifies the base memory address for memory accesses to the RTL8180 operational registers. This register must be initialized prior to accessing any RTL8180's register with memory access.

Bit	Symbol	Description
31:8	MEM31-8	**Base Memory Address:** This is set by software to the base address for the operational register map.
7:4	MEMSIZE	**Memory Size:** These bits return 0, which indicates that the RTL8180 requires 256 bytes of Memory Space.
3	MEMPF	**Memory Prefetchable:** Read only. Set to 0 by the RTL8180.
2:1	MEMLOC	**Memory Location Select:** Read only. Set to 0 by the RTL8180. This indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	**Memory Space Indicator:** Read only. Set to 0 by the RTL8180 to indicate that it is capable of being mapped into memory space.

CISPtr: CardBus CIS Pointer. This field is valid only when CardB_En (bit3, Config2) = 1. The value of this register is auto-loaded from 93C46 or 93C56 (from offset 50h-51h).

- Bit 2:0: Address Space Indicator

Bit2:0	Meaning
0	Not supported. (CIS begins in device-dependent configuration space.)
1:6	The CIS begins in the memory address governed by one of the six Base Address Registers. Ex. if the value is 2, then the CIS begins in the memory address space governed by Base Address Register 2.
7	The CIS begins in the Expansion ROM space.

- Bit27:3: Address Space Offset
- Bit31:28: ROM Image number

Bit2:0	Space Type	Address Space Offset Values
0	Configuration space	Not supported.
X; 1≤X≤6	Memory space	0h≤value≤FFFF FFF8h. This is the offset into the memory address space governed by Base Address Register X. Adding this value to the value in the Base Address Register gives the location of the start of the CIS. For RTL8180, the value is 100h.
7	Expansion ROM	0≤image number≤Fh, 0h≤value≤0FFF FFF8h. This is the offset into the expansion ROM address space governed by the Expansion ROM Base Register. The image number is in the uppermost nibble of the CISPtr register. The value consists of the remaining bytes. For RTL8180, the image number is 0h.

This read-only register points to where the CIS begins, in one of the following spaces:

i. Memory space – The CIS may be in any of the memory spaces from offset 100h and up after being auto-loaded from 93C56. The CIS is stored in 93C56 EEPROM physically from offset 80h-FFh.

ii. Expansion ROM space – The CIS is stored in expansion ROM physically within the 128KB max.

SVID: Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh, which is Realtek Semiconductor's PCI Subsystem Vendor ID.

SMID: Subsystem ID. This field will be set to value corresponding to PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8180h.

ILR: Interrupt Line Register

The Interrupt Line Register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8180.

IPR: Interrupt Pin Register

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8180. The RTL8180 uses INTA interrupt pin. Read only. IPR = 01h.

MNGNT: Minimum Grant Timer: Read only

Specifies how long a burst period the RTL8180 needs at 33 MHz clock rate in units of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

MXLAT: Maximum Latency Timer: Read only

Specifies how often the RTL8180 needs to gain access to the PCI bus in unit of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

8.6 Default Value After Power-on (RSTB Asserted)

PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	1	0	0	0	0	0	0	0
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	0	0	0	0	0	0	0
		W	-	PERRSP	-	MWIEN	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	1	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R/W	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		R/W	0	0	0	0	0	0	0	0
12h		R/W	0	0	0	0	0	0	0	0
13h		R/W	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		R/W	0	0	0	0	0	0	0	0
16h		R/W	0	0	0	0	0	0	0	0
17h		R/W	0	0	0	0	0	0	0	0
18h-27h	-	RESERVED(ALL 0)								
28h	CISPtr	R	0	0	0	0	0	0	0	0
29h		R	0	0	0	0	0	0	0	0
2Ah		R	0	0	0	0	0	0	0	0
2Bh		R	0	0	0	0	0	0	0	0
2Ch	SVID	R	1	1	1	0	1	1	0	0
2Dh		R	0	0	0	1	0	0	0	0
2Eh	SMID	R	1	0	0	0	0	0	0	0
2Fh		R	1	0	0	0	0	0	0	1
30h	BMAR	R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	BROMEN
31h		R	0	0	0	0	0	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	0	0	0	0	0	0	0	0
33h		R/W	0	0	0	0	0	0	0	0
34h	Cap-Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0
35h-3Bh	-	RESERVED(ALL 0)								
3Ch	ILR	R/W	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h-FFh	-	RESERVED(ALL 0)								

8.7 PCI Power Management Functions

The RTL8180 is compliant to ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), and Network Device Class Power Management Reference Specification (V1.0a), such as to support OS Directed Power Management (OSPM) environment. To support this, the RTL8180 provides the following capabilities:

- The RTL8180 can monitor the network for a Wakeup Frame, a Magic Packet, and notify the system via PME# when such a packet or event occurs. Then, the whole system can be restore to a working state to process the incoming jobs.

When the RTL8180 is in power down mode (D1 ~ D3):

- The Rx state machine is stopped, and the RTL8180 keeps monitoring the network for wakeup events such as Magic Packet, and Wakeup Frame in order to wake up the system. When in power down mode, the RTL8180 will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO.
- The FIFO status and the packets which are already received into Rx FIFO before entering into power down mode, are kept by the RTL8180 during power down mode.
- Transmission is stopped. The action of the PCI bus master mode is stopped as well. The Tx FIFO is kept.
- After restoration to a D0 state, the PCI bus master mode continues to transfer the data, which is not yet moved into the Tx FIFO from the last break. The packet that was not transmitted completely last time is transmitted again.

D3cold_support_PME bit(bit15, PMC register) & Aux_I_b2:0 (bit8:6, PMC register) in PCI configuration space.
If EEPROM D3cold_support_PME bit(bit15, PMC) = 1, the above 4 bits depend on the existence of Aux power.
If EEPROM D3cold_support_PME bit(bit15, PMC) = 0, the above 4 bits are all 0's.
Ex.:

1. If EEPROM D3c_support_PME = 1,
   - If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC, i.e. if EEPROM PMC = C2 F7, then PCI PMC = C2 F7.
   - If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. I.e. if EEPROM PMC = C2 F7, the PCI PMC = 02 76.
     - In this case, if wakeup support is desired when the main power is off, it is suggested that the EEPROM PMC be set to: C2 F7 (RT EEPROM default value).
2. If EEPROM D3c_support_PME = 0,
   - If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC. I.e. if EEPROM PMC = C2 77, then PCI PMC = C2 77.
   - If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's. I.e. if EEPROM PMC = C2 77, the PCI PMC = 02 76.
     - In this case, if wakeup support is not desired when the main power is off, it is suggested that the EEPROM PMC be set to be 02 76.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8180, such as broadcast, multicast, or unicast address to the current RTL8180 adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC(can be none)+ 16 * DID(Destination ID) in any part of a valid packet.

Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8180, such as broadcast, multicast, or unicast address to the current RTL8180 adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The **16-bit CRC*** (or **16-bit CRC**) of the received Wakeup Frame matches with the **16-bit CRC*** of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8180 is configured to allow direct packet wakeup, such as broadcast, multicast, or unicast network packet.

  - **16-bit CRC:**

    The RTL8180 supports 5 wakeup frames that includes 2 normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and 3 long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The PME# signal is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8180 may assert PME# in D1, D2 and D3 power state, or the RTL8180 is in isolation state, referring to PME_Support(bit15-11) of the PMC register in PCI Configuration Space.
- Magic Packet, or Wakeup Frame has occurred.
  - Writing a 1 to the PME_Status (bit15) of PMCSR register in the PCI Configuration Space will clear this bit and cause the RTL8180 to stop asserting a PME# (if enabled).

When the RTL8180 is in power down mode, ex. D1-D3, the IO and MEM spaces are all disabled, after a RST# assertion, the RTL8180's power state is restored to D0 automatically, if the original power state is $D3_{cold}$. There is no hardware delay at the RTL8180's power state transition. When in ACPI mode, the RTL8180 does not support PME from D0 (This is Realtek default setting of PMC register autoloaded from EEPROM. The setting may be changed from the EEPROM, if required.).

8.8 VPD (Vital Product Data)

Bit 31 of VPD is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56 is completed or not.

1. Write VPD register: (write data to 93C46/93C56)
   Write the flag bit to a one (at the same time the VPD address is written). When the flag bit is set to zero by the RTL8180, the VPD data (all 4 bytes) has been transferred from the VPD data register to 93C46/93C56.
2. Read VPD register: (read data from 93C46/93C56)
   Write the flag bit to a zero at the same time the VPD address is written). When the flag bit is set to one by the RTL8180, the VPD data (all 4 bytes) has been transferred from 93C46/93C56 to the VPD data register.

9. Functional Description

9.1 Transmit & Receive Operations

The RTL8180 supports a new descriptor-based buffer management that will significantly lower host CPU utilization. The RTL8180 supports up to 64 consecutive descriptors in memory for transmit and receive separately, which means there might be 5 descriptor rings. Transmit descriptor rings have one beacon transmit descriptor ring, one high priority descriptor ring, one normal priority descriptor ring and one low priority descriptor ring. Each transmit descriptor ring may consist of up to 64 8-double-word consecutive descriptors and each receive descriptor ring may consist of up to 64 4-double-word consecutive descriptors, separately. The start address of each descriptor group should be in 256-byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet, in both Tx and Rx. Please refer to the Realtek RTL8180 programming guide for detailed information. Any Tx buffers pointed to by one of the Tx descriptors should be at least 4 bytes.

9.1.1 Transmit

The following information describes what the Tx descriptor may look like, depending on different states in each Tx descriptor. The minimum Tx buffer should be at least 4 bytes.

9.1.1.1 Tx Descriptor Format (before transmitting, OWN=1, Tx command mode 1)

bit 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

OWN=1	RSVD	FS	LS	TXRATE (4 bits)				RTSEN	RTSRATE (4 bits)				BEACON	MOREFRAG	SPLCP	KEY ID		RSVD		TPKTSIZE (12 bits)											Offset 0
LENGEXT	Length (15 bits)															RTSDUR (16 bits)															Offset 4
TX_BUFFER_ADDRESS																															Offset 8
RSVD (20 bits)																				Frame_Length(12 bits)											Offset 12
NEXT_TX_DESCRIPTOR_ADDRESS																															Offset 16
RSVD																															Offset 20
RSVD																															Offset 24
RSVD																															Offset 28

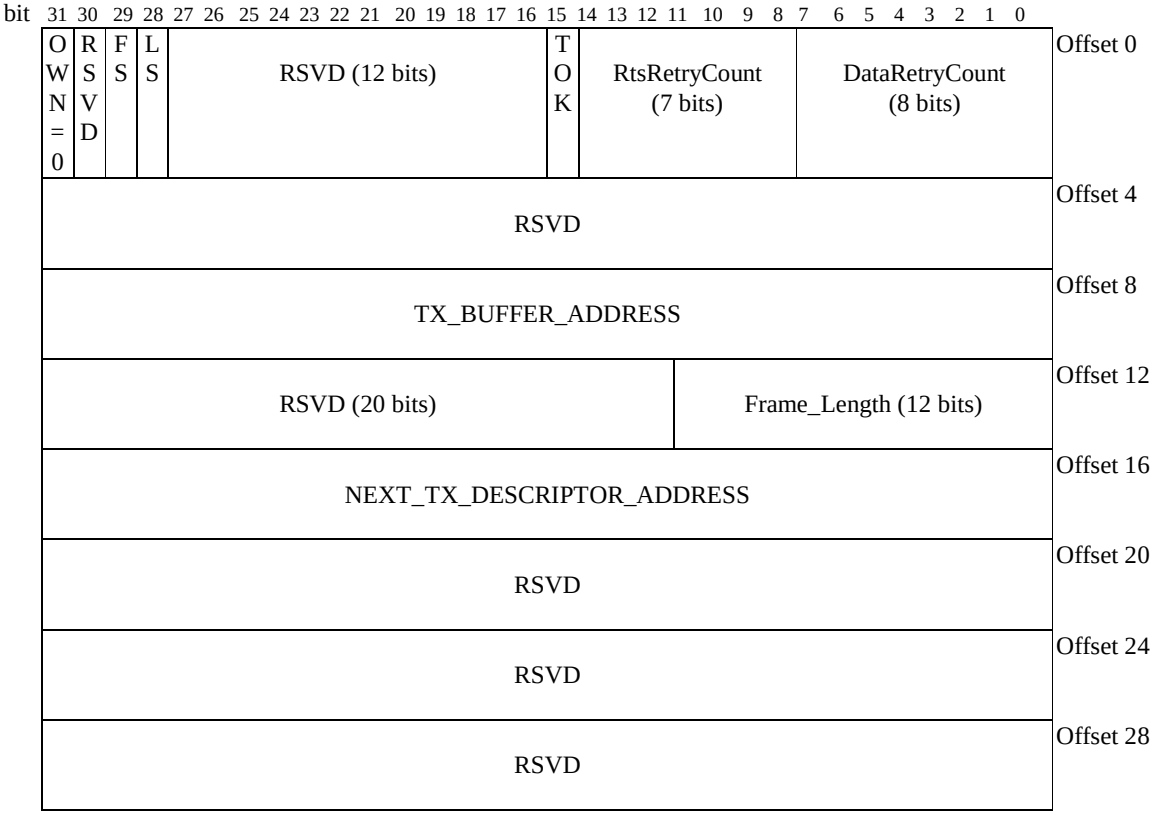
<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>OWN</td><td>Ownership: When set, this bit indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.</td></tr>
<tr><td>0</td><td>30</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>0</td><td>29</td><td>FS</td><td>First Segment Descriptor: When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.</td></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last Segment Descriptor: When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27:24</td><td>TXRATE</td><td>Tx Rate: These four bits indicate the current frame’s transmission rate.
<table>
<tr><th></th><th>Bit 27</th><th>Bit 26</th><th>Bit 25</th><th>Bit 24</th></tr>
<tr><td>1 Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2 Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>5.5 Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11 Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="4">All other combinations</td></tr>
</table></td></tr>
<tr><td>0</td><td>23</td><td>RTSEN</td><td>RTS Enable: This bit set to 1 indicates that an RTS/CTS handshake shall be performed at the beginning of any frame exchange sequence where the frame is a Data or Management type, the frame has a unicast address in the Address1 field, and the length of the frame is greater than RTSThreshold.</td></tr>
<tr><td>0</td><td>22:19</td><td>RTSRATE</td><td>RTS Rate: These four bits indicate the RTS frame’s transmission rate before transmitting the current frame and will be ignored if the RTSEN bit is set to 0.
<table>
<tr><th></th><th>Bit 22</th><th>Bit 21</th><th>Bit 20</th><th>Bit 19</th></tr>
<tr><td>1 Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2 Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>5.5 Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11 Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="4">All other combinations</td></tr>
</table></td></tr>
<tr><td>0</td><td>18</td><td>BEACON</td><td>Beacon Frame: This bit set to 1 to indicates that this frame is beacon frame.</td></tr>
<tr><td>0</td><td>17</td><td>MOREFRAG</td><td>More Fragment: This bit is set to 1 in all data type frames that have another fragment of the current packet to follow.</td></tr>
</table>

Cont…

<table>
<tr><td>0</td><td>16</td><td>SPLCP</td><td>Short PLCP format: When set, this bit indicates that it needed to add a short PLCP preamble and header format before transmitting the frame.</td></tr>
<tr><td>0</td><td>15:14</td><td>KEYID</td><td>Key ID: The key ID selects one of four possible secret key values for use in encrypting this frame.
<table>
<tr><th></th><th>Bit 15</th><th>Bit 14</th></tr>
<tr><td>Default Key 0</td><td>0</td><td>0</td></tr>
<tr><td>Default Key 1</td><td>0</td><td>1</td></tr>
<tr><td>Default Key 2</td><td>1</td><td>0</td></tr>
<tr><td>Default Key 3</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>0</td><td>13:12</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>0</td><td>11:0</td><td>TPKTSIZE</td><td>Transmit Packet Size: This field indicates the number of bytes required to transmit the frame.</td></tr>
<tr><td>4</td><td>31</td><td>LENGEXT</td><td>Length Extension: This bit is used to supplement the Length field (bits 30:16, offset 4). This bit will be ignored if the TXRATE is set to 1Mbps or 2Mbps.</td></tr>
<tr><td>4</td><td>30:16</td><td>Length</td><td>PLCP Length: The PLCP length field indicates the number of microseconds required to transmit the frame.</td></tr>
<tr><td>4</td><td>15:0</td><td>RTSDUR</td><td>RTS Duration: These bits indicate the RTS frame’s duration field before transmitting the current frame and will be ignored if the RTSEN bit is set to 0.</td></tr>
<tr><td>8</td><td>31:0</td><td>TxBuff</td><td>32-bit Address of Transmit Buffer</td></tr>
<tr><td>12</td><td>31:12</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>12</td><td>11:0</td><td>Frame_Length</td><td>Transmit Frame Length: This field indicates the length in the Tx buffer, in bytes, to be transmitted.</td></tr>
<tr><td>16</td><td>31:0</td><td>NTDA</td><td>32-bit Address of Next Transmit Descriptor Address</td></tr>
<tr><td>20</td><td>31:0</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>24</td><td>31:0</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>28</td><td>31:0</td><td>RSVD</td><td>Reserved</td></tr>
</table>

9.1.1.2 Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

After having transmitted, the Tx descriptor turns into a Tx status descriptor.



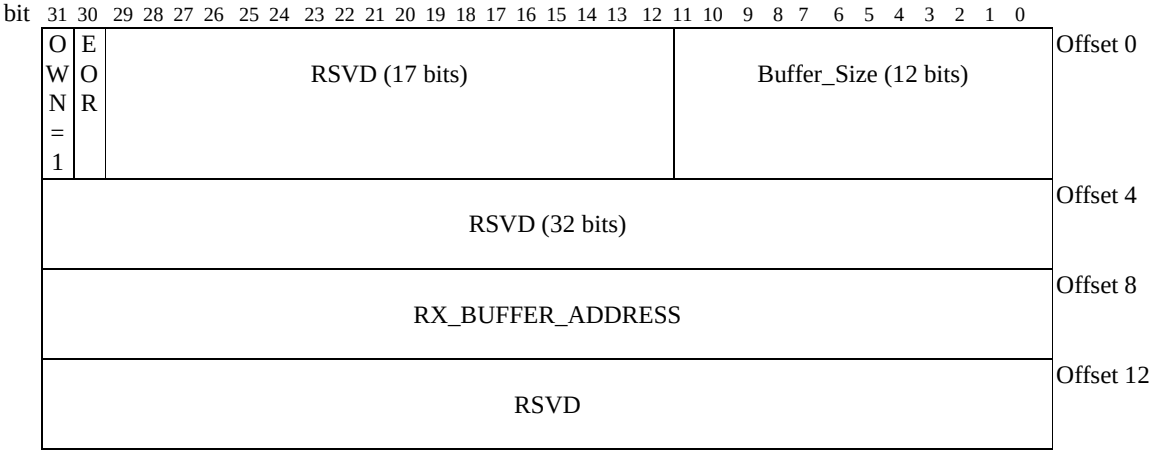
Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, this bit indicates that the descriptor is owned by the NIC. When clear, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is already transmitted. In this case, OWN=0.
0	30	RSVD	**Reserved**
0	29	FS	**First Segment Descriptor:** When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** When set, this bit indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27:16	RSVD	**Reserved**
0	15	TOK	**Transmit (Tx) OK:** Indicates that a packet exchange sequence is completed successfully.
0	14:8	RTSRetry	**RTS packet retry count.**
0	7:0	DRC	**Data packet Retry Count:** The RC's initial value is 0. It indicates the number of retrys when a packet is transmitted complete.
4	31:0	RSVD	**Reserved**
8	31:0	TxBuff	**32-bit Address of Transmit Buffer**
12	31:12	RSVD	**Reserved**
12	11:0	Frame_Length	**Transmit Frame Length:** This field indicates the length in the Tx buffer, in bytes, to be transmitted.
16	31:0	NTDA	**32-bit Address of Next Transmit Descriptor Address**
20	31:0	RSVD	**Reserved**
24	31:0	RSVD	**Reserved**
28	31:0	RSVD	**Reserved**

9.1.2 Receive

The following describes what the Rx descriptor may look like, depending on different states in each Rx descriptor. Any Rx buffer pointed to by one of the Rx descriptors should be at least 4 bytes.

9.1.2.1 Rx Command Descriptor (OWN=1)

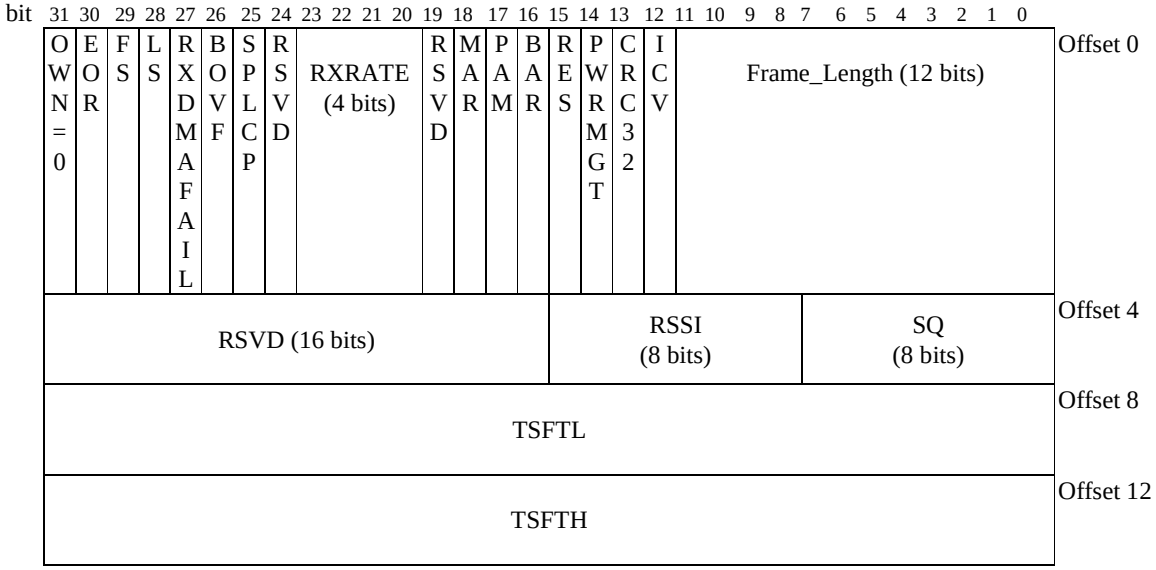
The driver should pre-allocate Rx buffers and configure Rx descriptors before packet reception. The following describes what a Rx descriptor may look like before packet reception.



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, this bit indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated a buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	**End of Rx Descriptor Ring:** This bit set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29:12	RSVD	**Reserved**
0	11:0	Buffer_Size	**Buffer Size:** This field indicate the receive buffer size in bytes.
4	31:0	RSVD	**Reserved**
8	31:0	RxBuff	**32-bit Address of Receive Buffer**
12	31:0	RSVD	**Reserved**

9.1.2.2 Rx Status Descriptor (OWN=0)

When packet is received, the Rx command descriptor turns to be a Rx status descriptor.



Offset#	Bit#	Symbol	Description
0	31	OWN	**Ownership:** When set, this bit indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the NIC has filled this Rx buffer with a packet or part of a packet. In this case, OWN=0.
0	30	EOR	**End of Rx Descriptor Ring:** This bit set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29	FS	**First Segment Descriptor:** When set, this bit indicates that this is the first descriptor of a received packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	**Last Segment Descriptor:** When set, this bit indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.
0	27	RXDMAFAIL	**RX DMA Fail:** When set, this bit indicates that a receive DMA failure has occurred on the received packet.
0	26	BOVF	**Buffer Overflow:** When set, this bit indicates that a receive buffer has exhausted before this packet is received.
0	25	SPLCP	**Short PLCP format:** When set, this bit indicates that the current received frame has added short PLCP preamble and header format.
0	24	RSVD	**Reserved**
0	23:20	RXRATE	**Rx Rate:** These four bits indicate the current frame's receiving rate.

	Bit 23	Bit 22	Bit 21	Bit 20
1 Mbps	0	0	0	0
2 Mbps	0	0	0	1
5.5 Mbps	0	0	1	0
11 Mbps	0	0	1	1
Reserved	All other combinations			

Cont…

0	19	RSVD	**Reserved**
0	18	MAR	**Multicast Address Packet Received:** When set, this bit indicates that a multicast packet is received.
0	17	PAM	**Physical Address Matched:** When set, this bit indicates that the destination address of this Rx packet matches the value in the RTL8180's ID registers.
0	16	BAR	**Broadcast Address Received:** When set, this bit indicates that a broadcast packet is received. BAR and MAR will not be set simultaneously.
0	15	RES	**Receive Error Summary:** When set, this bit indicates that at least one of the following errors has occurred: CRC32, ICV. This bit is valid only when LS (the Last Segment bit) is set.
0	14	PWRMGT	**Receive Power Management Packet:** When set, this bit indicates that the Power Management bit is set on the received packet.
0	13	CRC32	**CRC32 Error:** When set, this bit indicates that a CRC32 error has occurred on the received packet. A CRC32 packet can be received only when RCR_ACRC32 is set.
0	12	ICV	**ICV Error:** When set, this bit indicates that an ICV error has occurred on the received packet. A ICV packet can be received only when RCR_AICV is set.
0	11:0	Frame_Length	When OWN=0 and LS =1, this bit indicates the received packet length including CRC32, in bytes.
4	31:16	RSVD	**Reserved**
4	15:8	RSSI	**Received Signal Strength Indicator:** The RSSI is a measure of the RF energy received by the PHY.
4	7:0	SQ	**Signal Quality:** The SQ is a measure of the quality of BAKER code lock, providing an effective measure during the full reception of a PLCP preamble and header.
8	31:0	TSFTL	A snapshot of the TSFTR's least significant 32 bits. Valid only when LS is set.
12	31:0	TSFTH	A snapshot of the TSFTR's most significant 32 bits. Valid only when LS is set.

9.2 Loopback Operation

Loopback mode is normally used to verify that the logic operations have performed correctly. In loopback mode, the RTL8180 takes frames from the transmit descriptor and transmits them up to internal Rx logic. The loopback function does not apply to an external PHYceiver.

9.3 Tx Encapsulation

With RTL8180 Internal Baseband Processor

While operating in Tx mode, the RTL8180 encapsulates the frames that it transmits according to the Differential Binary Phase Shift Keying (DBPSK) for 1Mbps, Differential Quaternary Phase Shift Keying (DQPSK) for 2Mbps, and Complementary Code Keying (CCK) for 5.5Mbps and 11Mbps modulators. The changes of the original packet data are listed as follows:

1. The PLCP preamble is always transmitted as the DBPSK waveform and used by the receiver to achieve initial PN synchronization.
2. The PLCP header can be configured to be either DBPSK or DQPSK and includes the necessary data fields of the communications protocol to establish the physical layer link.
3. The MAC frame can be configured for DBPSK, DQPSK or CCK.

9.4 Rx Decapsulation

With RTL8180 Internal Baseband Processor

The RTL8180 continuously monitors the network when reception is enabled. When activity is recognized it starts to process the incoming data. After detecting receive activity on the channel, the RTL8180 starts to process the PLCP preamble and header based on the mode of operation.

The RTL8180 checks CRC16 and CRC32, then reports if CRC16 and CRC32 has error. The RTL8180 also checks the ICV when using the 40-bit WEP and 104-bit WEP module to decrypt and reports if ICV has errors.

9.5 Memory Functions

9.5.1 Memory Read Line (MRL)

The Memory Read Line command reads more than a longword (DWORD), up to the cache line boundary, in a prefetchable address space. The Memory Read Line command is semantically identical to the Memory Read command except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by reading up to a cache line boundary in response to the request rather than a single memory cycle. As with the Memory Read command, pre-fetched buffers must be invalidated before any synchronization events are passed through this access path.

The RTL8180 performs MRL according to the following rules:

i. Read access that reaches the cache line boundary uses the Memory Read Line command (MRL), instead of Memory Read command.

ii. Read access that does not reach the cache line boundary uses Memory Read (MR) command.

iii. Memory Read Line (MRL) command operates in conjunction with Memory Read Multiple command (MRM).

iv. RTL8180 will terminate the read transaction on the cache line boundary when it is out of resources on the transmit DMA. For example, the transmit FIFO is almost full.

9.5.2 Memory Read Multiple (MRM)

The Memory Read Multiple command is semantically identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The memory controller should continue pipelining memory requests as long as FRAMEB is asserted. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by sequentially reading ahead one or more additional cache line(s) when a software transparent buffer is available for temporary storage.

The RTL8180 performs MRM according to the following rules:

i. When RTL8180 reads full cache lines, it will use Memory Read Multiple command.

ii. If the memory buffer is not cache-aligned, the RTL8180 will use Memory Read Line command to reach the cache line boundary first.

Example:

Assume the packet length = 1514 byte, cache line size = 16 longwords (DWORDs), and Tx buffer start address = 64m+4 (m > 0).

;Step1: Memory Read Line (MRL)
;Data: (0-3) => (4-7) => (8-11) =>……... => (56-59) (byte offset of the Tx packet)
;From Address: <64m+4>, <64m+8>, ……., <64m+60> (reach cache line boundary)
;Step2. Memory Read Multiple (MRM)
;Data: (60-63) => (64-67) => (68-71) => ……..….. => (1454-1467)
;From Address: <64m+64>, <64m+68>, ……..…., <64m+64+(16*4)*21+(16-1)*4>
;Step3. Memory Read(MR)
;Data: (1468-1471) => (1472-1475) => ……, => (1510-1513)
;From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>
Step1: Memory Read Multiple (MRM)
Data: (0-3) => (4-7) => (8-11) =>…….. => (1454-1467)
From Address: <64m+4>, <64m+8>, ……., <64m+64+(16*4)*21+(16-1)*4>
Step2. Memory Read(MRL)
Data: (1468-1471) => (1472-1475) => ……, => (1510-1513)
From Address:<64m+64+(16*4)*22>,<64m+64+(16*4)*22+4>,..,<64m+64+(16*4)*22+42>

9.5.3 Memory Write and Invalidate (MWI)

The Memory Write and Invalidate command is semantically identical to the Memory Write command except that it additionally guarantees a minimum transfer of one complete cache line; i.e., the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. Note: All byte enables must be asserted during each data phase for this command. The master may allow the transaction to cross a cache line boundary only if it intends to transfer the entire next line also. This command requires implementation of a configuration register in the master indicating the cache line size and may only be used with Linear Burst Ordering. It allows a memory performance optimization by invalidating a "dirty" line in a write-back cache without requiring the actual write-back cycle, thus shortening access time. The RTL8180 uses MWI command while writing full cache lines, and Memory Write command while writing partial cache lines.

When the following requirements are approved, the RTL8180 issues MWI command, instead of MW command on Rx DMA.

i. The Cache Line Size written in the offset 0Ch of the PCI configuration space is 8 or 16 longwords (DWORDs).

ii. The accessed address is cache line aligned.

iii. The RTL8180 has at least 8/16 longwords (DWORDs) of data in its RX FIFO.

iv. The MWI (bit 4) in the PCI configuration command register should be set to 1.

The RTL8180 uses the Memory Write(MW) command instead of MWI whenever there's any one of the above listed requirements failed. The RTL8180 terminates the WMI cycle at the end of the cache line when a WMI cycle has started and at least one of the requirements are no longer hold.

Example:

Assume Rx packet length = 1514 byte, cache line size = 16 DWORDs (longwords), and Rx buffer start address = 64m+4 (m > 0).

Step1: Memory Write (MW)
Data: (0-3) => (4-7) => (8-11) => ……... => (56-59) (byte offset of the Rx packet)
To Address: <64m+4>, <64m+8>, ……., <64m+60> (reach cache line boundary)
Step2. Memory Write and Invalidate (MWI)
Data: (60-63) => (64-67) => (68-71) => ……..…..... => (1454-1457)
To Address: <64m+64>, <64m+68>, ……..….., <64m+64+(16*4)*21+(16-1)*4>
Step3. Memory Write(MW)
Data: (1458-1461) => (1462-1465) => ……..……... => (1512-1513)
To Address: <64m+64+(16*4)*22>, <64m+64+(16*4)*22+4>, , <64m+64+(16*4)*22+42>

9.6 LED Functions

The RTL8180 supports 2 LED signals in 4 different configurable operation modes. The following sections describe the different LED actions.

9.6.1 Link Monitor

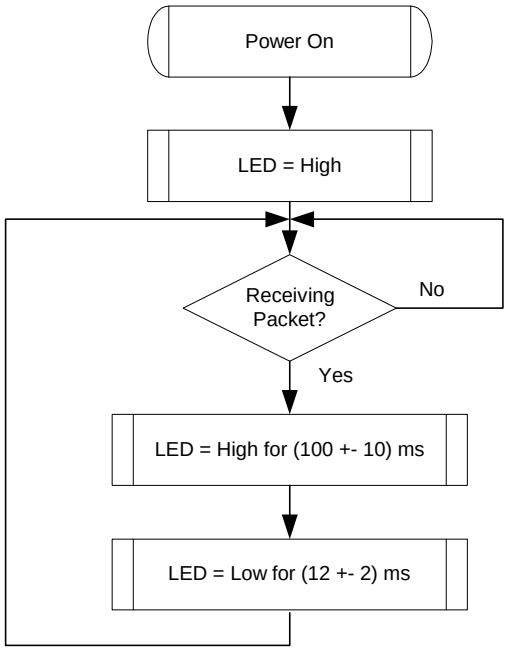
The Link Monitor senses the link integrity. Whenever link status is established, the specific link LED pin is driven low.

9.6.2 Infrastructure Monitor

The Infrastructure Monitor senses the link integrity at Infrastructure network. Whenever link ok at Infrastructure network status is established, the specific Infrastructure LED pin is driven low.

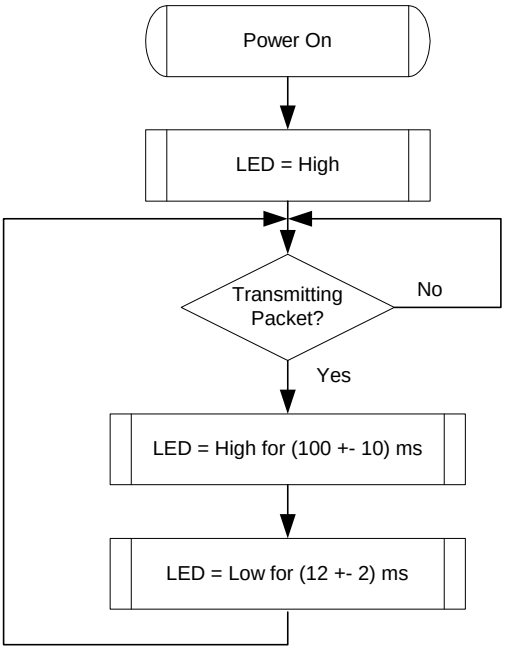
9.6.3 Rx LED

Blinking of the Rx LED indicates that receive activity is occurring.



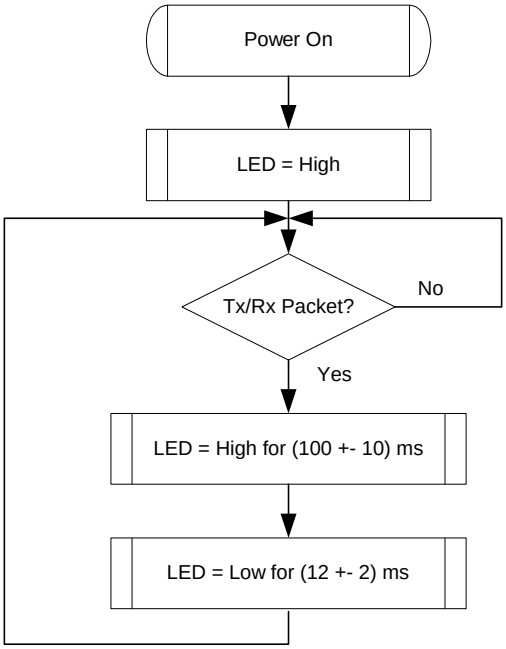
9.6.4 Tx LED

Blinking of the Tx LED indicates that transmit activity is occurring.



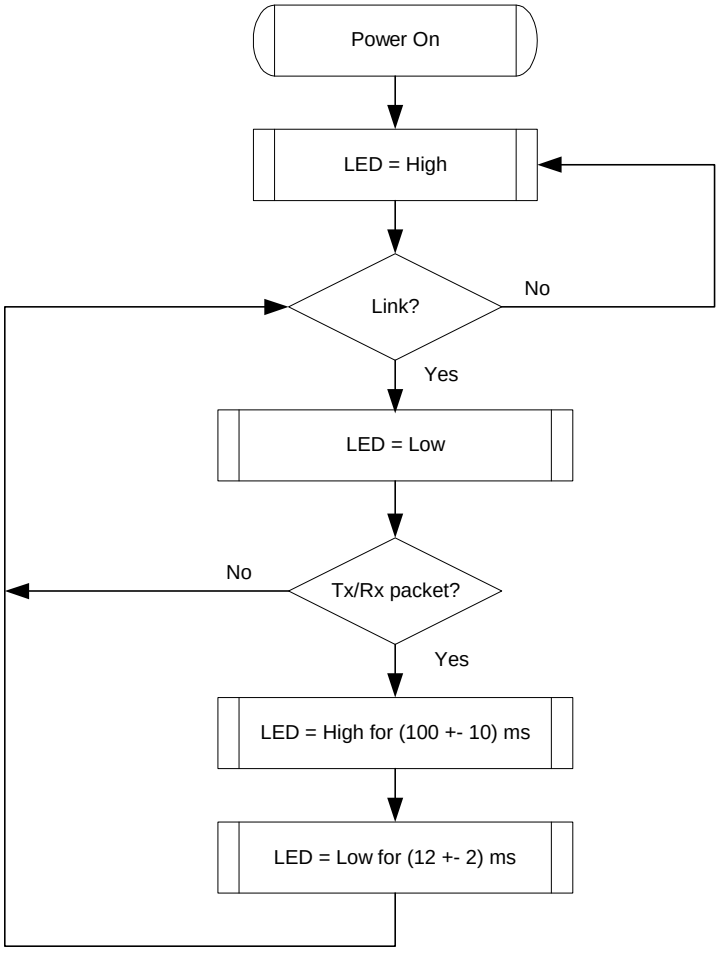
9.6.5 Tx/Rx LED

Blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

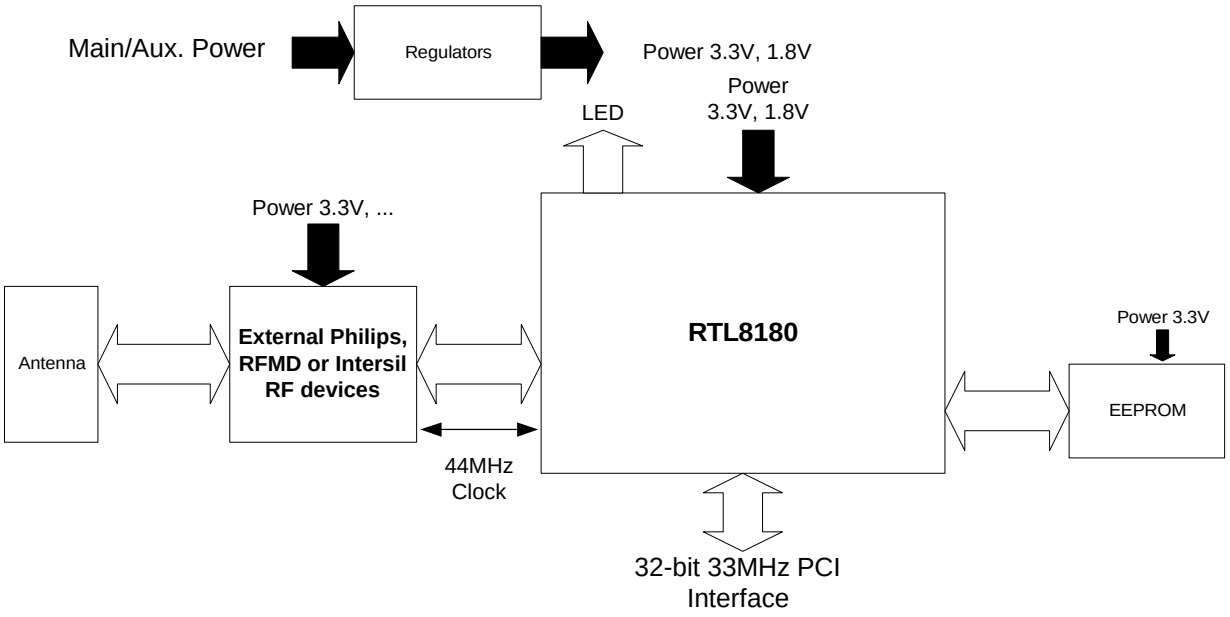


9.6.6 LINK/ACT LED

Blinking of the LINK/ACT LED indicates that the RTL8180 is linked and operating properly. This LED high for extended periods, indicates that a link problem exists.



10. Application Diagram



11. Electrical Characteristics

11.1 Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	°C
Operating temperature	0	70	°C

11.2 DC Characteristics

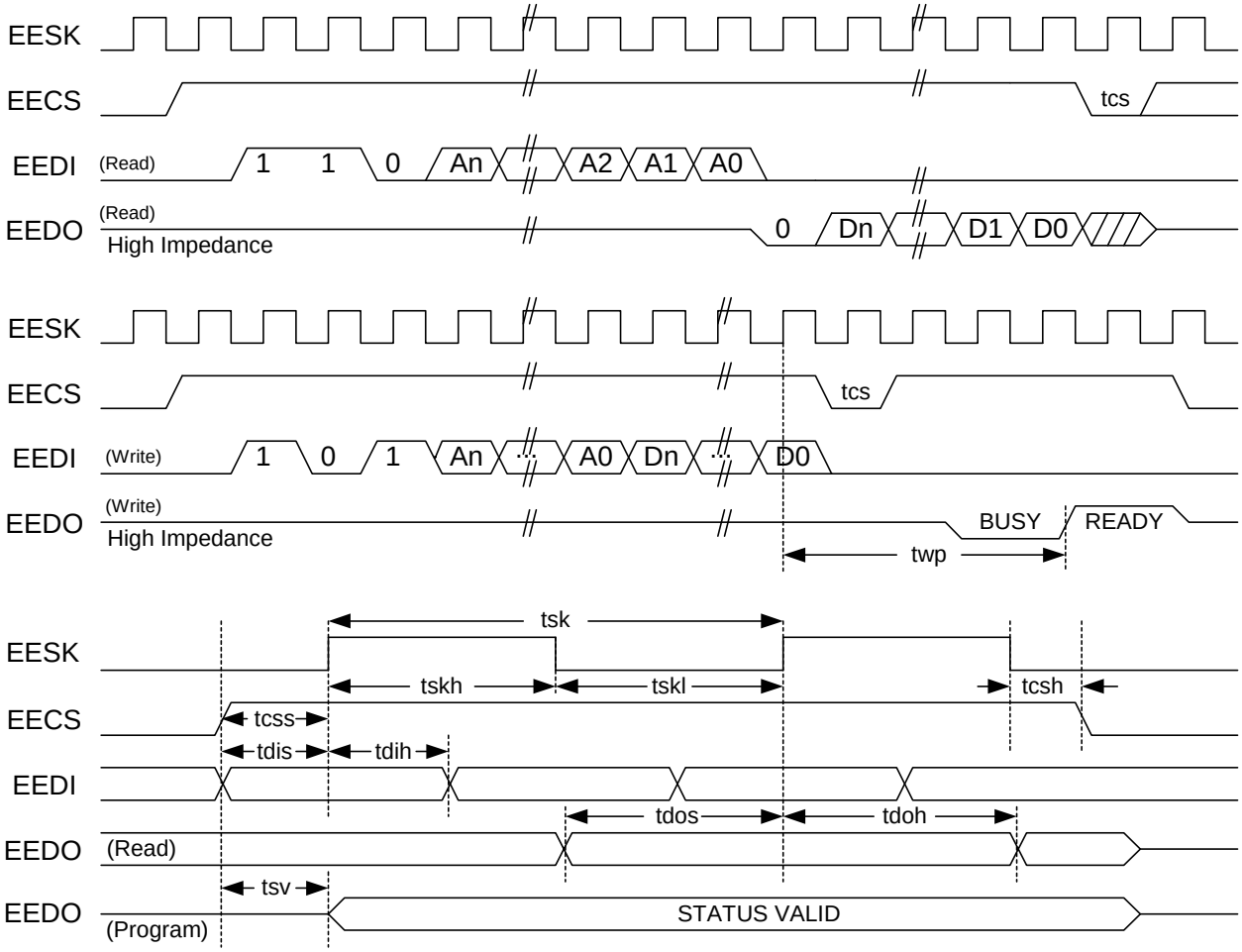
Below is a description of the general DC specifications for the RTL8180.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage		3.0	3.3	3.6	V
VDD18	1.8V Supply Voltage		1.7	1.8	1.9	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -8mA	0.9 * Vcc		Vcc	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 8mA			0.1 * Vcc	V
V_{ih}	Minimum High Level Input Voltage		0.5 * Vcc		Vcc+0.5	V
V_{il}	Maximum Low Level Input Voltage		-0.5		0.3 * Vcc	V
I_{in}	Input Current	V_{in} =V_{cc} or GND	-1.0		1.0	μA
I_{oz}	Tri-State Output Leakage Current	V_{out} =V_{cc} or GND	-10		10	μA
I_{cc}	Average Operating Supply Current	I_{out} = 0mA,			330	mA

11.3 AC Characteristics

11.3.1 Serial EEPROM Interface Timing

(93C46(64*16)/93C56(128*16))



Symbol	Parameter		Minimum	Typical	Maximum	Units
tcs	Minimum CS Low Time	9346/9356	1000/250			ns
twp	Write Cycle Time	9346/9356			10/10	ms
tsk	SK Clock Cycle Time	9346/9356	4/1			µs
tskh	SK High Time	9346/9356	1000/500			ns
tskl	SK Low Time	9346/9356	1000/250			ns
tcss	CS Setup Time	9346/9356	200/50			ns
tcsh	CS Hold Time	9346/9356	0/0			ns
tdis	DI Setup Time	9346/9356	400/50			ns
tdih	DI Hold Time	9346/9356	400/100			ns
tdos	DO Setup Time	9346/9356	2000/500			ns
tdoh	DO Hold Time	9346/9356			2000/500	ns
tsv	CS to Status Valid	9346/9356			1000/500	ns

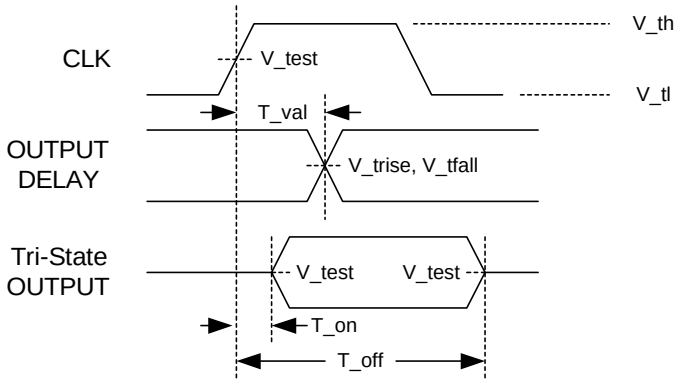
EEPROM Access Timing Parameters

11.3.2 PCI Bus Operation Timing

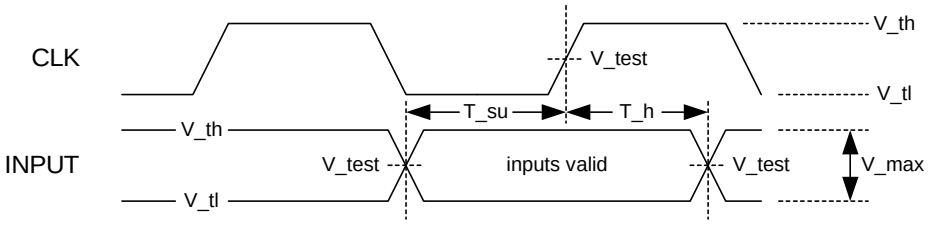
PCI Bus Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
T val	CLK to Signal Valid Delay-bused signals	2	11	ns
T val(ptp)	CLK to Signal Valid Delay-point to point	2	12	ns
T on	Float to Active Delay	2		ns
T off	Active to Float Delay		28	ns
T su	Input Setup Time to CLK-bused signals	7		ns
T su(ptp)	Input Setup Time to CLK-point to point	10		ns
T h	Input Hold Time from CLK	0		ns
T rst	Reset active time after power stable	1		ms
T rst-clk	Reset active time after CLK STABLE	100		µs
T rst-off	Reset Active to Output Float delay		40	ns
T rhfa	RSTB High to First configuration Access	2^25		clocks
T rhff	RSTB High to First FRAMEB assertion	5		clocks

PCI Interface Timing Parameters



Output Timing Measurement Condition

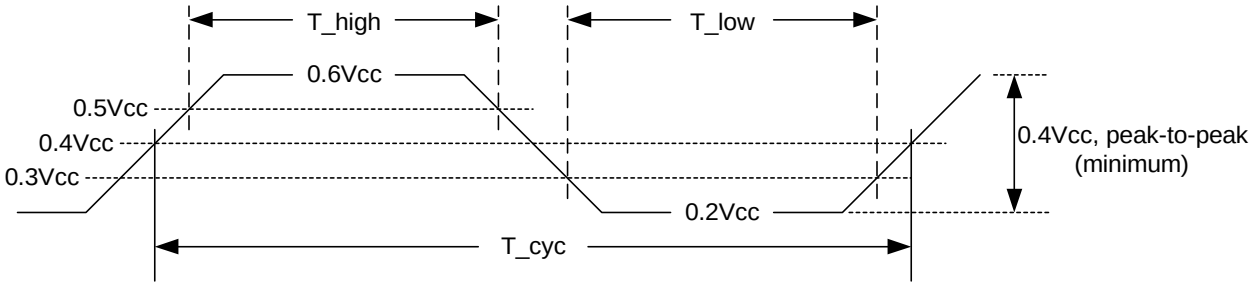


Input Timing Measurement Conditions

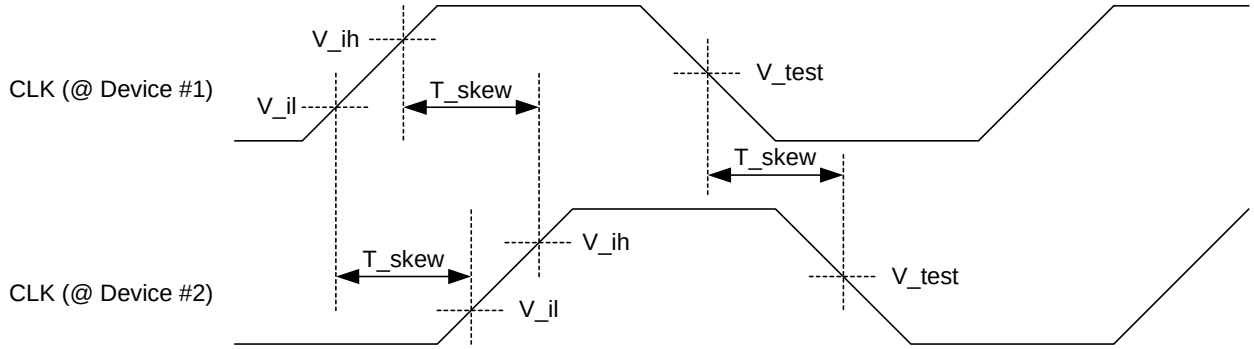
Symbol	Level	Units
Vth	0.6Vcc	V
Vtf	0.2Vcc	V
Vtest	0.4Vcc	V
Vtrise	0.285Vcc	V
Vtfall	0.615Vcc	V
Vmax	0.4Vcc	V
Input Signal Edge Rate	1	V/ns

Measurement Condition Parameters

PCI Clock Specification



Clock Waveform

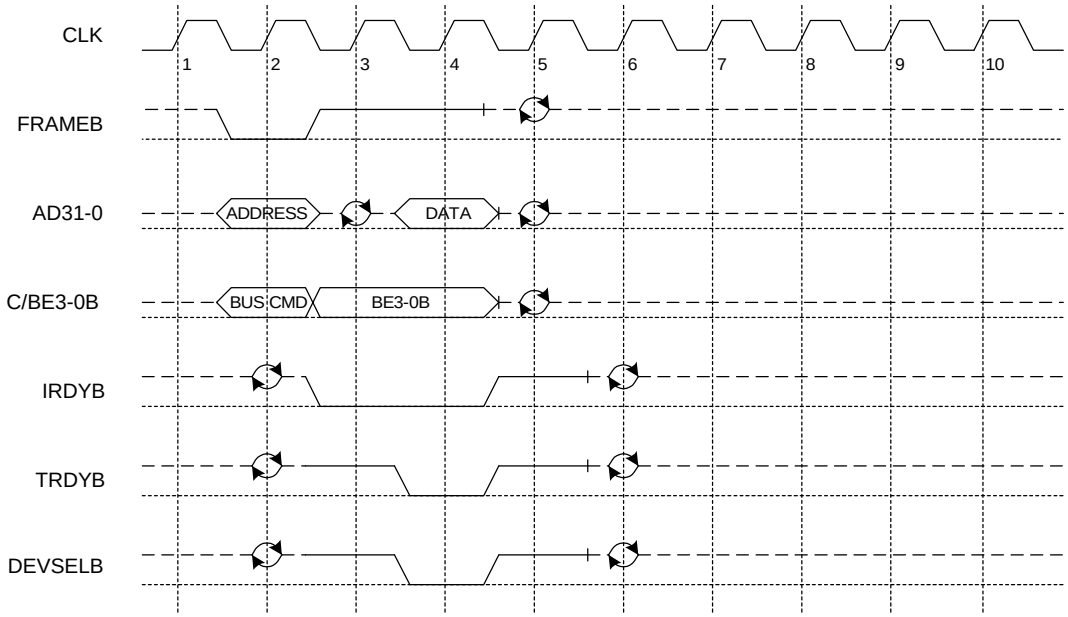


Clock Skew Diagram

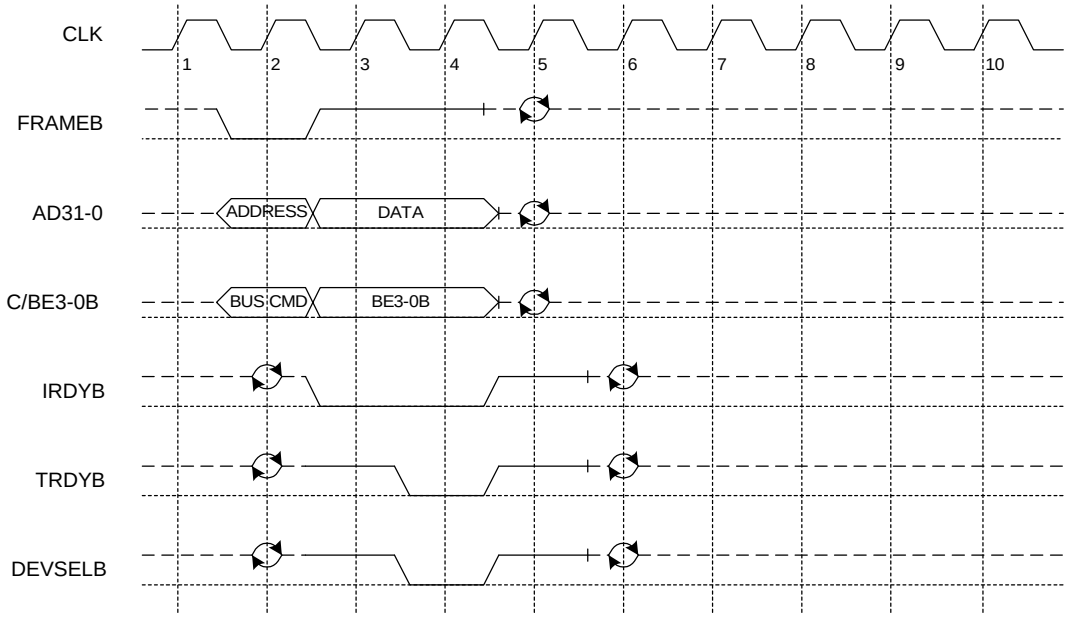
Symbol	Parameter	Minimum	Maximum	Units
Tcyc	**CLK** Cycle Time	30	∞	ns
Thigh	**CLK** High Time	11		ns
Tlow	**CLK** Low Time	11		ns
--	**CLK** Slew Rate	1	4	V/ns
--	**RST#** Slew Rate	50	-	mV/ns
Tskew	**CLK** Skew		2	ns

Clock and Reset Specifications

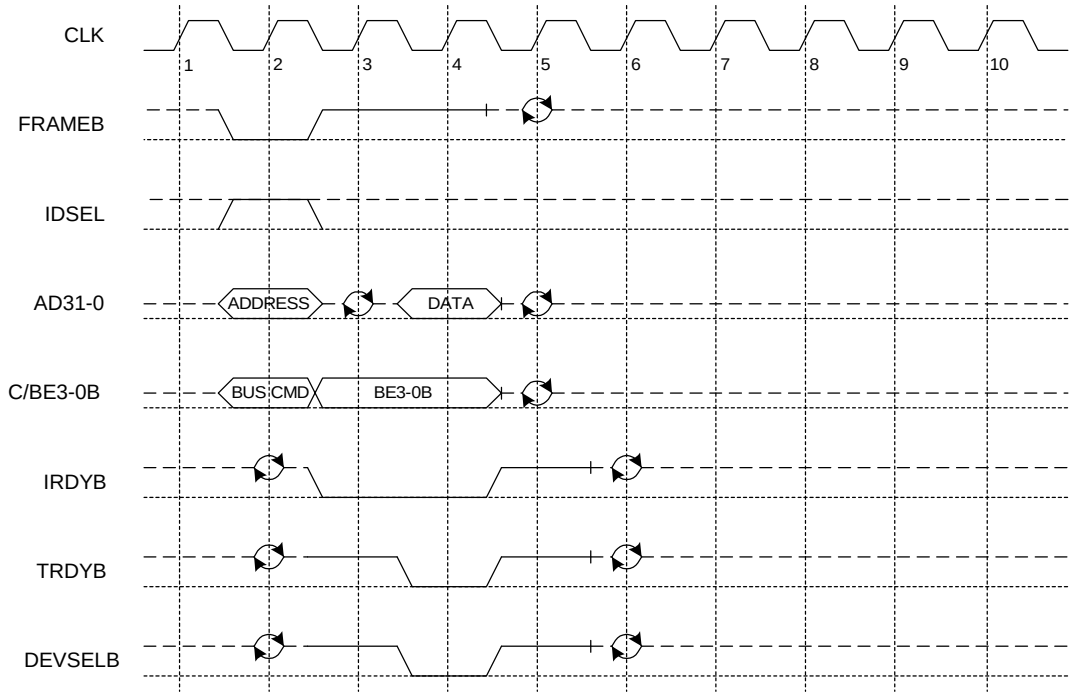
PCI Transactions



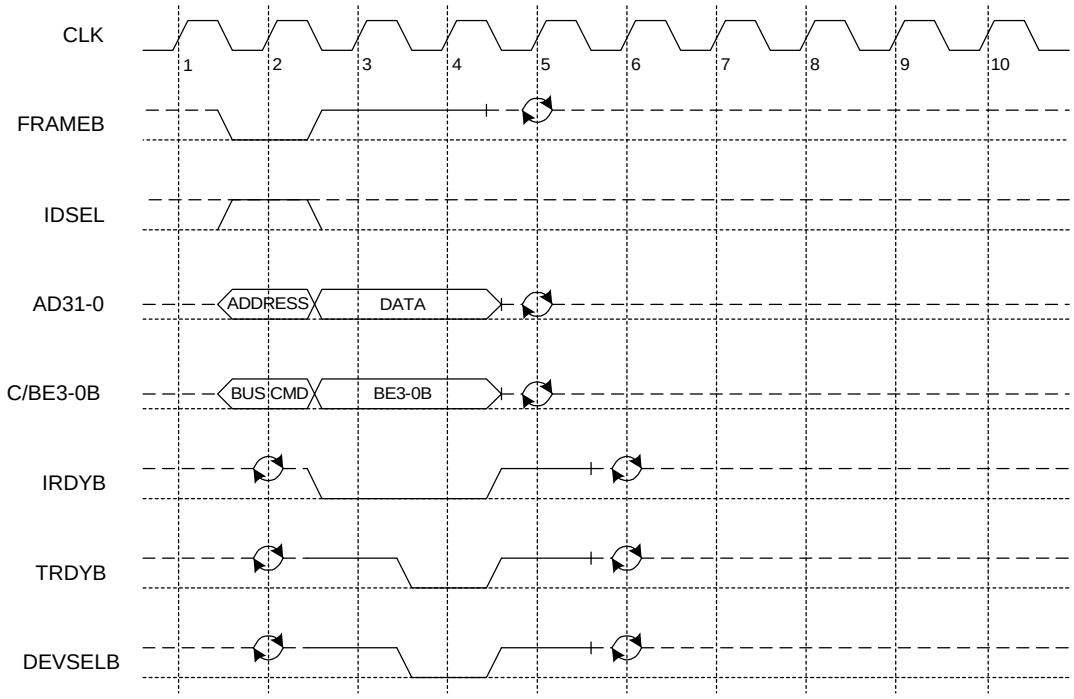
I/O Read



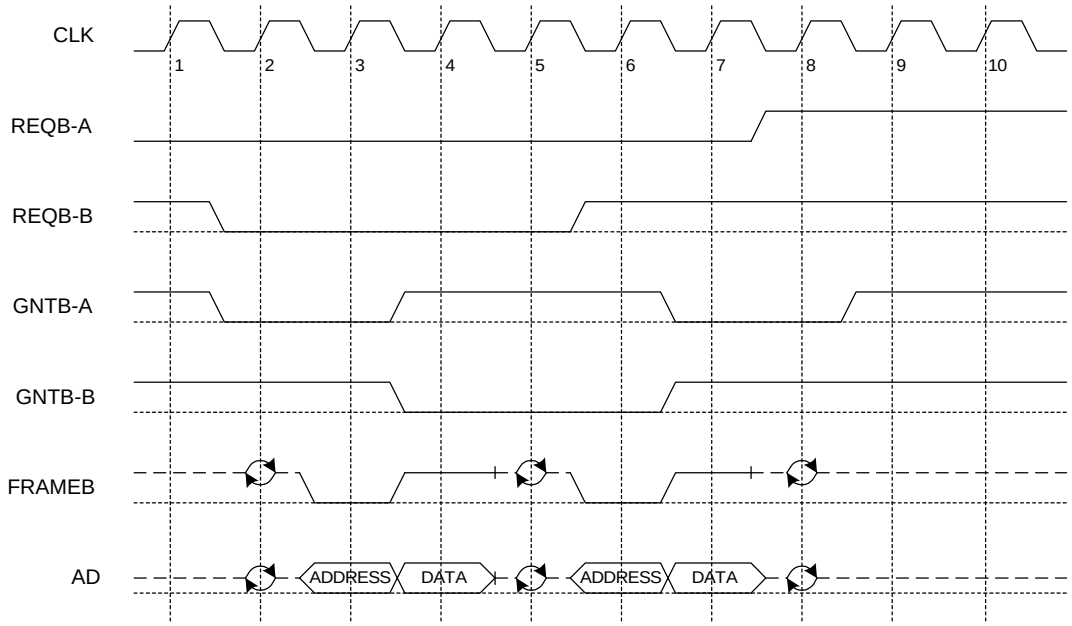
I/O Write



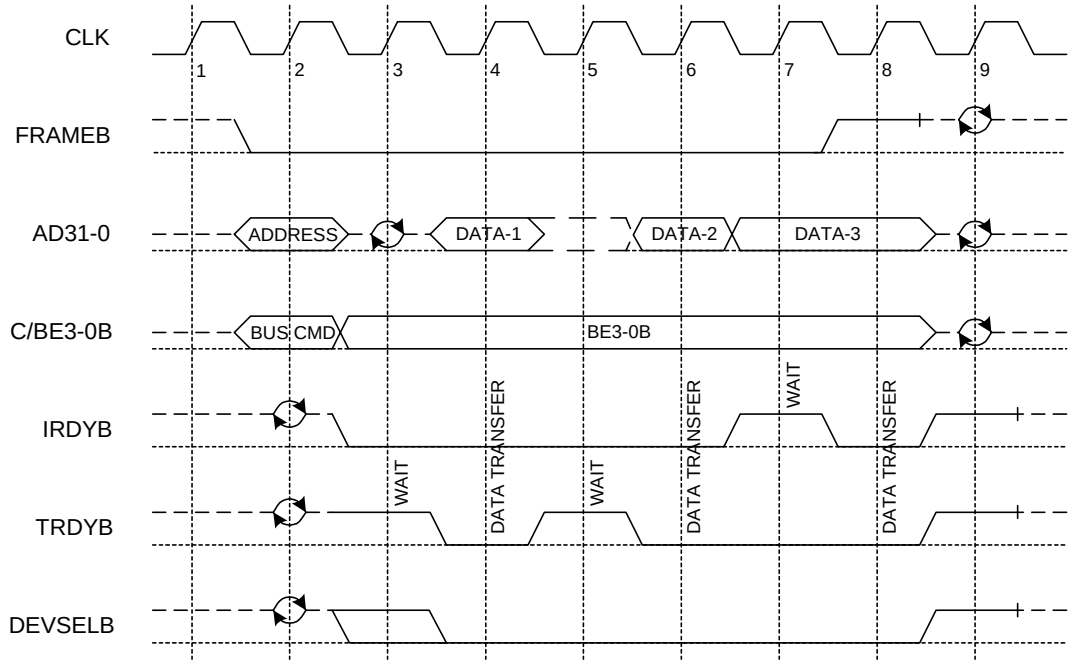
Configuration Read



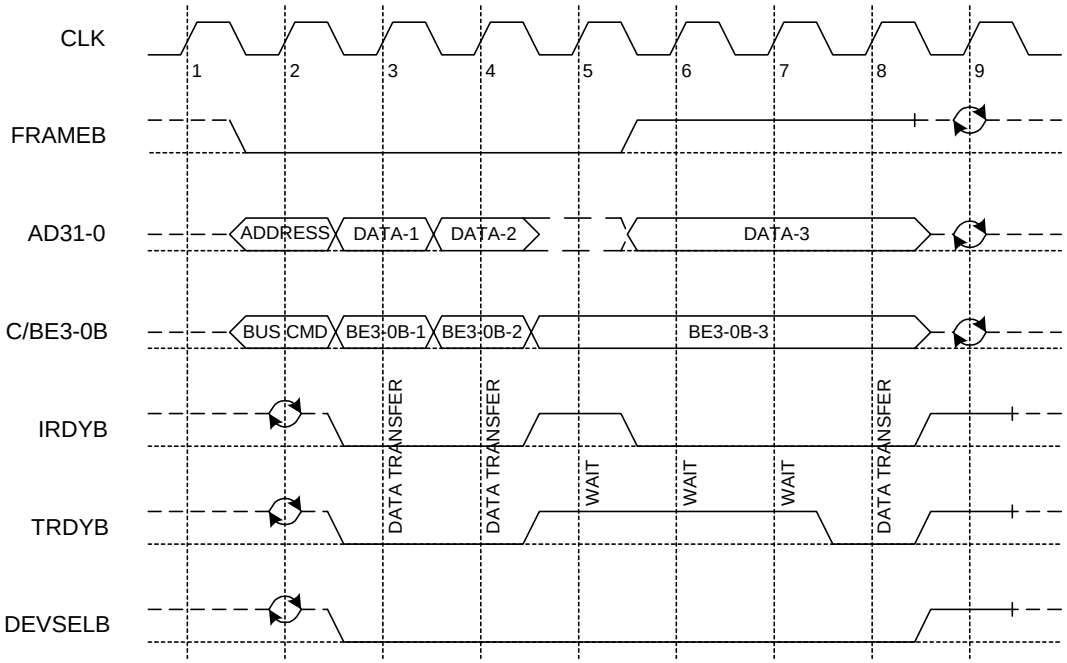
Configuration Write



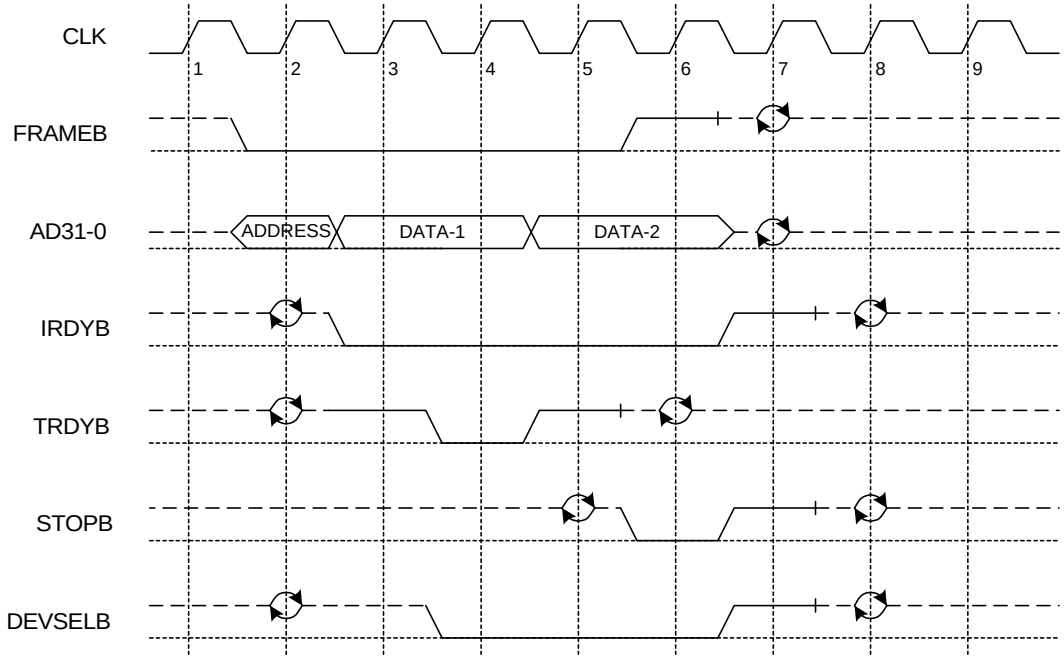
BUS Arbitration



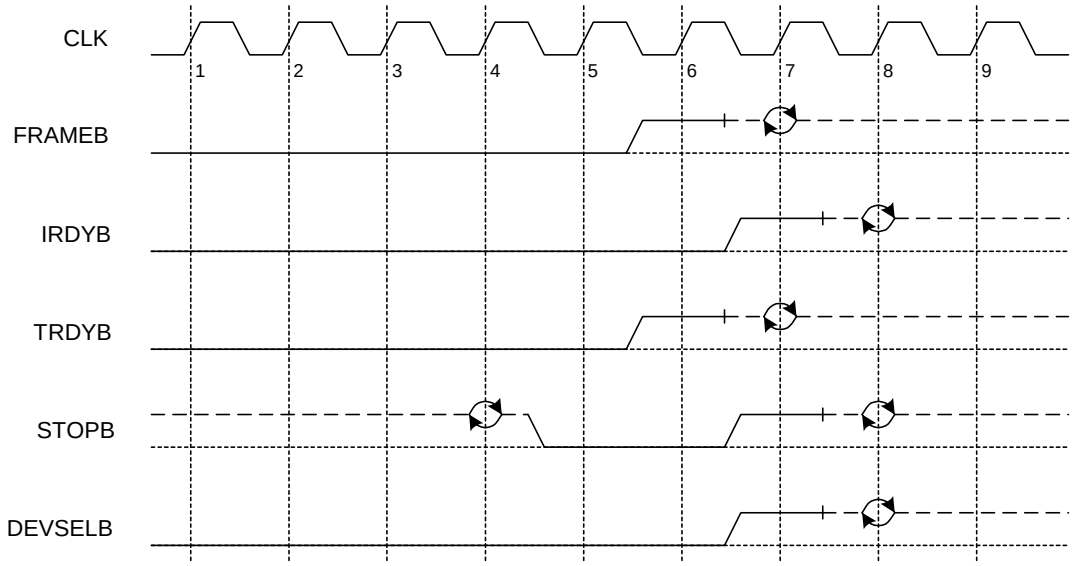
Memory Read



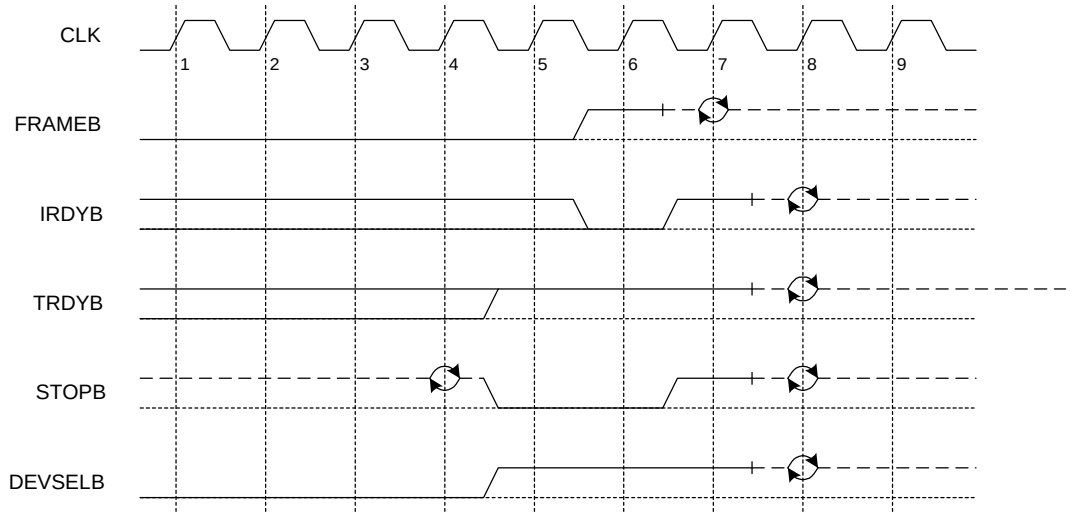
Memory Write



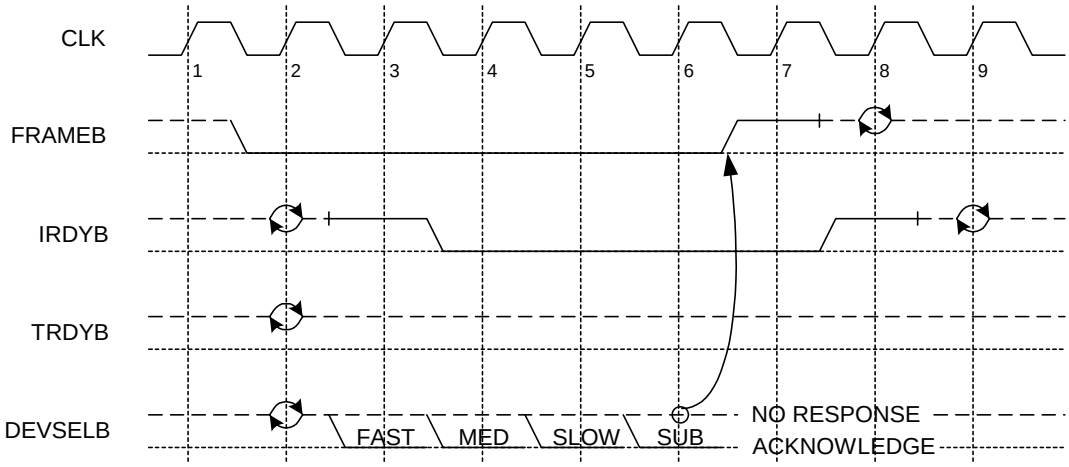
Target Initiated Termination - Retry



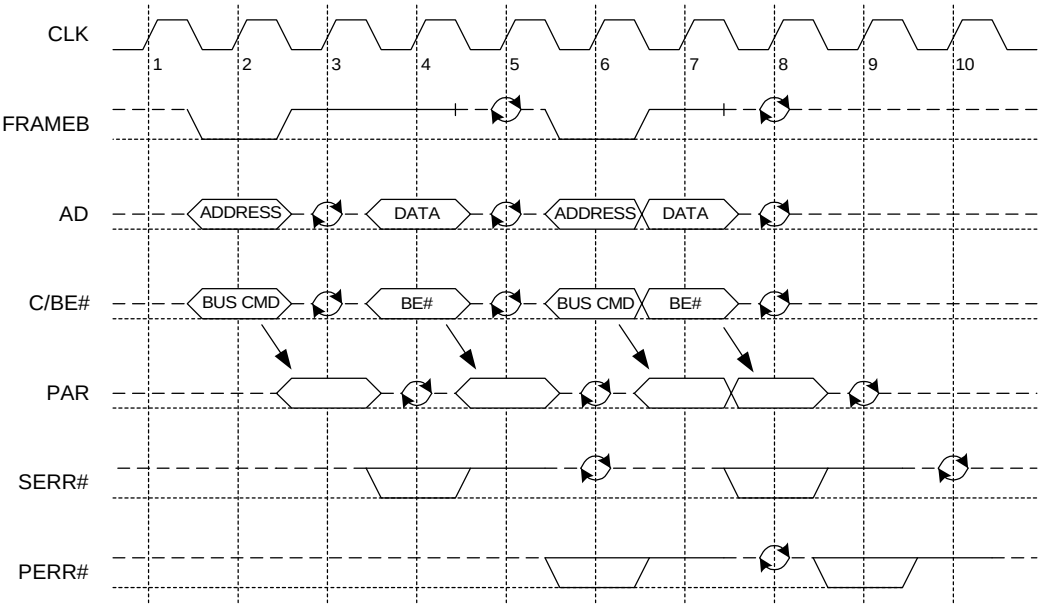
Target Initiated Termination - Disconnect



Target Initiated Termination - Abort

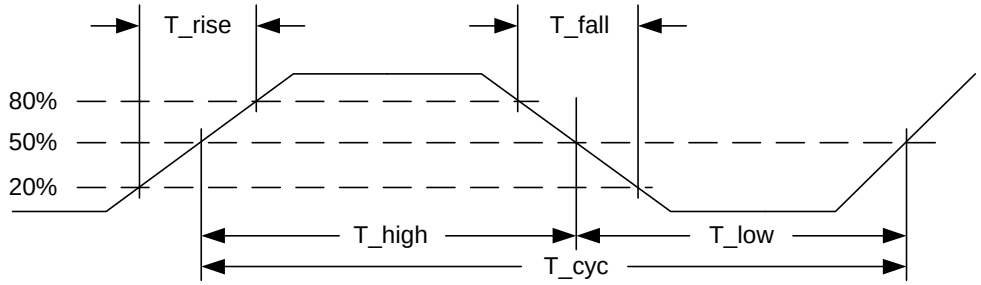


Master Initiated Termination - Abort

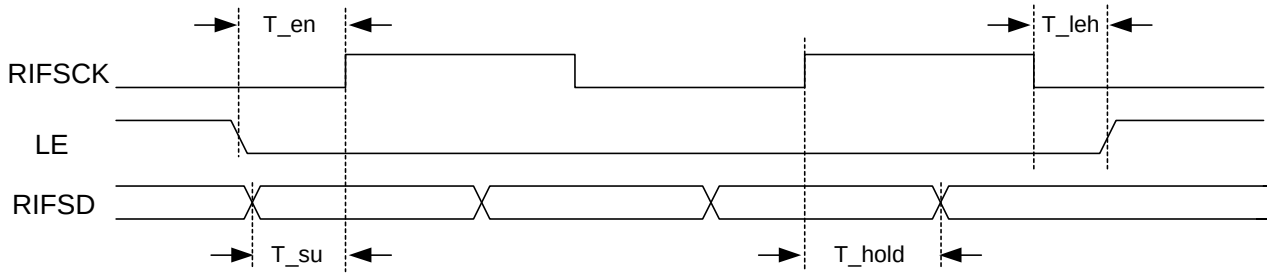


Parity Operation - One Example

11.3.3 Serial Interface Timing



Clock Waveform



Serial Interface Timing Didgram

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_cyc	RIFSCK Cycle Time	40			ns
T_rise	RIFSCK Rise Time			40	ns
T_fall	RIFSCK Fall Time			40	ns
T_high	RIFSCK High Time	20			ns
T_low	RIFSCK Low Time	20			ns
T_su	RIFSD Setup Time	20			ns
T_hold	RIFSD Hold Time	10			ns
T_sv	LE to Status Valid	10			ns
T_leh	LE Hold Time	20			ns

Serial Interface Timin Parameters

First bit																			**Last bit**
B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
Data Field																		**Register Definition**	

Intersil Chipset Serial Data Format

First bit																					**Last bit**
D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
Data Field																		**Address Field**			

RFMD Chipset Serial Data Format

First bit

A0	A1	A2	A3	A4	A5	A6	R/W	D0	D1	D2	D3	D4	D5	D6	D7
Address Field							R/W	**Data Field**							

Last bit

D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23
Data Field															

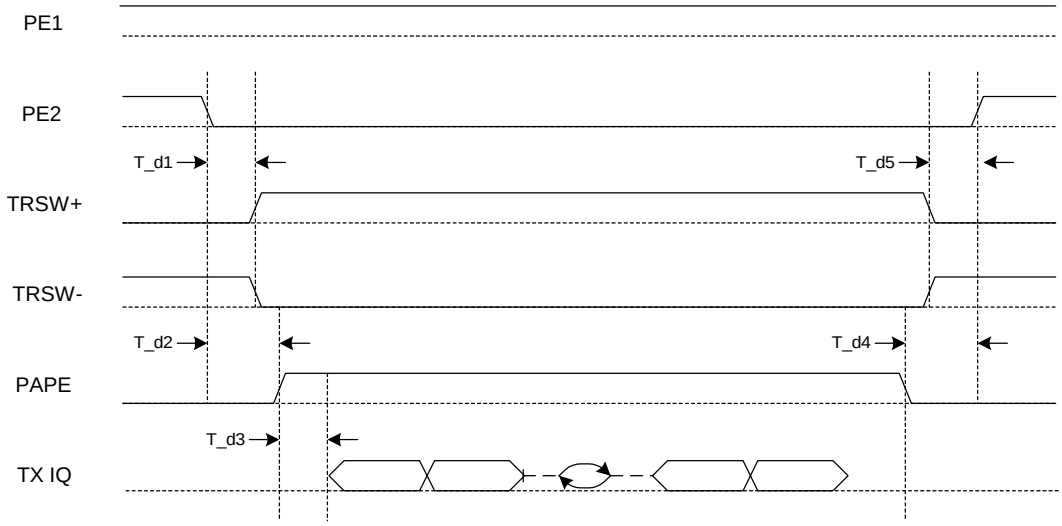
Philips Chipset Serial Data Format

Note: For programming serial control register, please refer to Intersil, RFMD and Philips' data sheet.

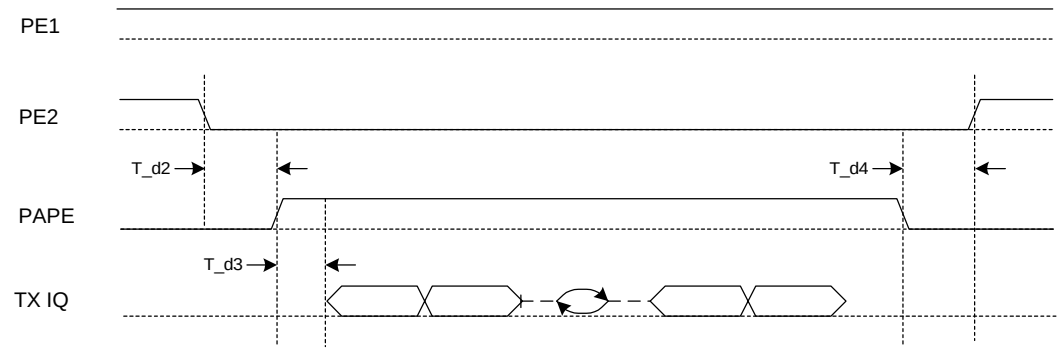
11.3.4 RF Control Timing

Symbol	Parameter	Delay	Tolerance	Units
T_d1	PE2 to TRSW	2	±0.1	µs
T_d2	PE2 to PAPE	3	±0.1	µs
T_d3	PAPE to TXIQ	Controlled by PAPE_sign (bit 2, Config 2) and PAPE_time (bits 1:0, Config 2)	±0.1	µs
T_d4	PAPE to PE2	3	±0.1	µs
T_d5	TRSW to PE2	2	±0.1	µs

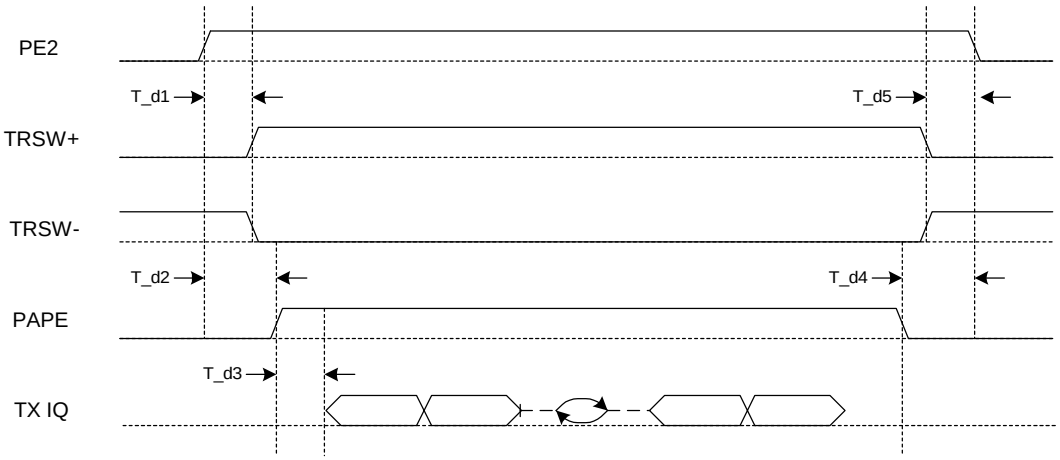
Transmit Control Timing Specifications



Transmit Control Signal Sequencing of Intersil Chipset

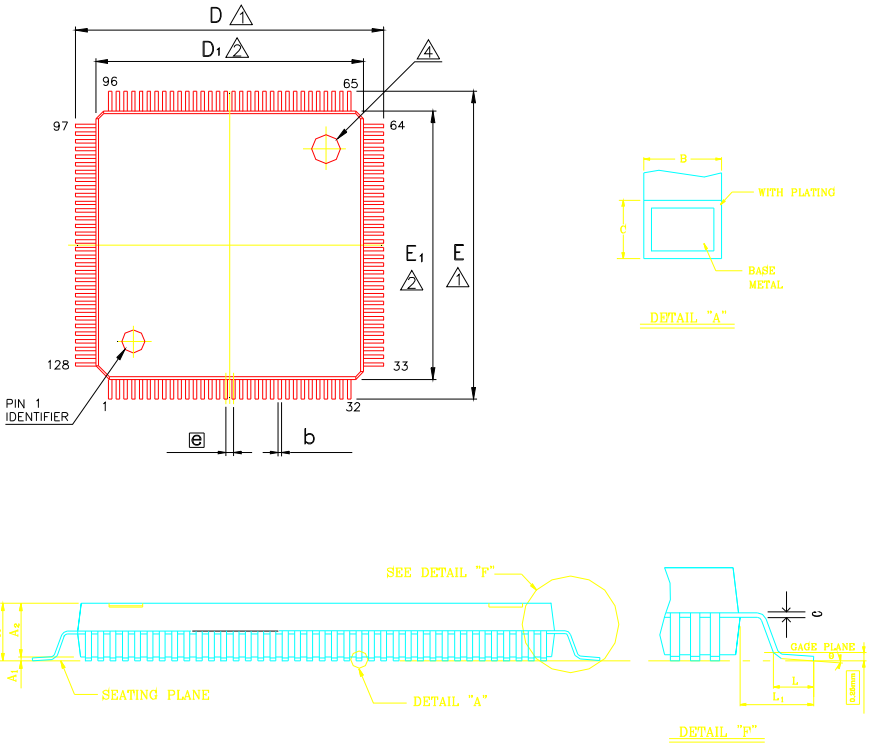


Transmit Control Signal Sequencing of RFMD Chipset



Transmit Control Signal Sequencing of Philips Chipset

12. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.063	-	-	1.60
A1	0.002	-	-	0.05	-	-
A2	0.053	0.055	0.057	1.35	**1.40**	1.45
b	0.005	0.007	0.009	0.13	**0.18**	0.23
c	0.004	-	0.006	0.09	-	0.20
D	0.624	0.630	0.636	15.85	**16.00**	16.15
D1	0.547	0.551	0.555	13.90	**14.00**	14.10
e	0.016 BSC			0.40 BSC		
E	0.624	0.630	0.636	15.85	**16.00**	16.15
E1	0.547	0.551	0.555	13.90	**14.00**	14.10
L	0.018	0.024	0.030	0.45	**0.60**	0.75
L1	0.039 REF			1.00 REF		
Θ	0°	3.5°	7°	0°	3.5°	7°

Note:
1. Dimension b does not include dambar protrusion/intrusion.
2. Controlling dimension: Millimeter
3. General appearance spec. should be based on final visual inspection spec.

TITLE: 128LD LQFP (14x14x1.4 mm*2) PACKAGE OUTLINE -CU L/F, FOOTPRINT 2.0 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	LQ128 - 2
		DATE	MAY. 13.2002
REALTEK SEMI-CONDUCTOR CO., LTD			

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